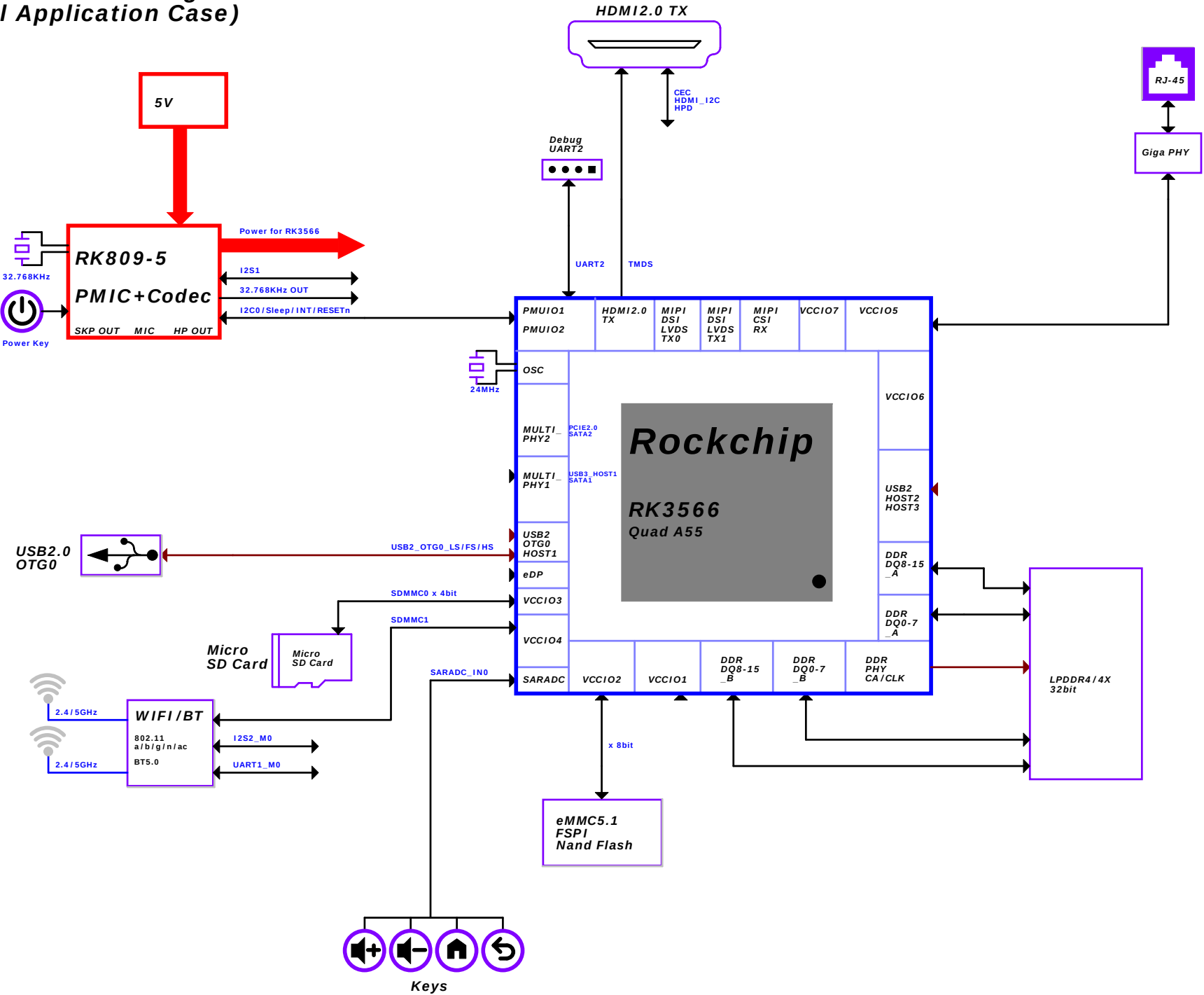
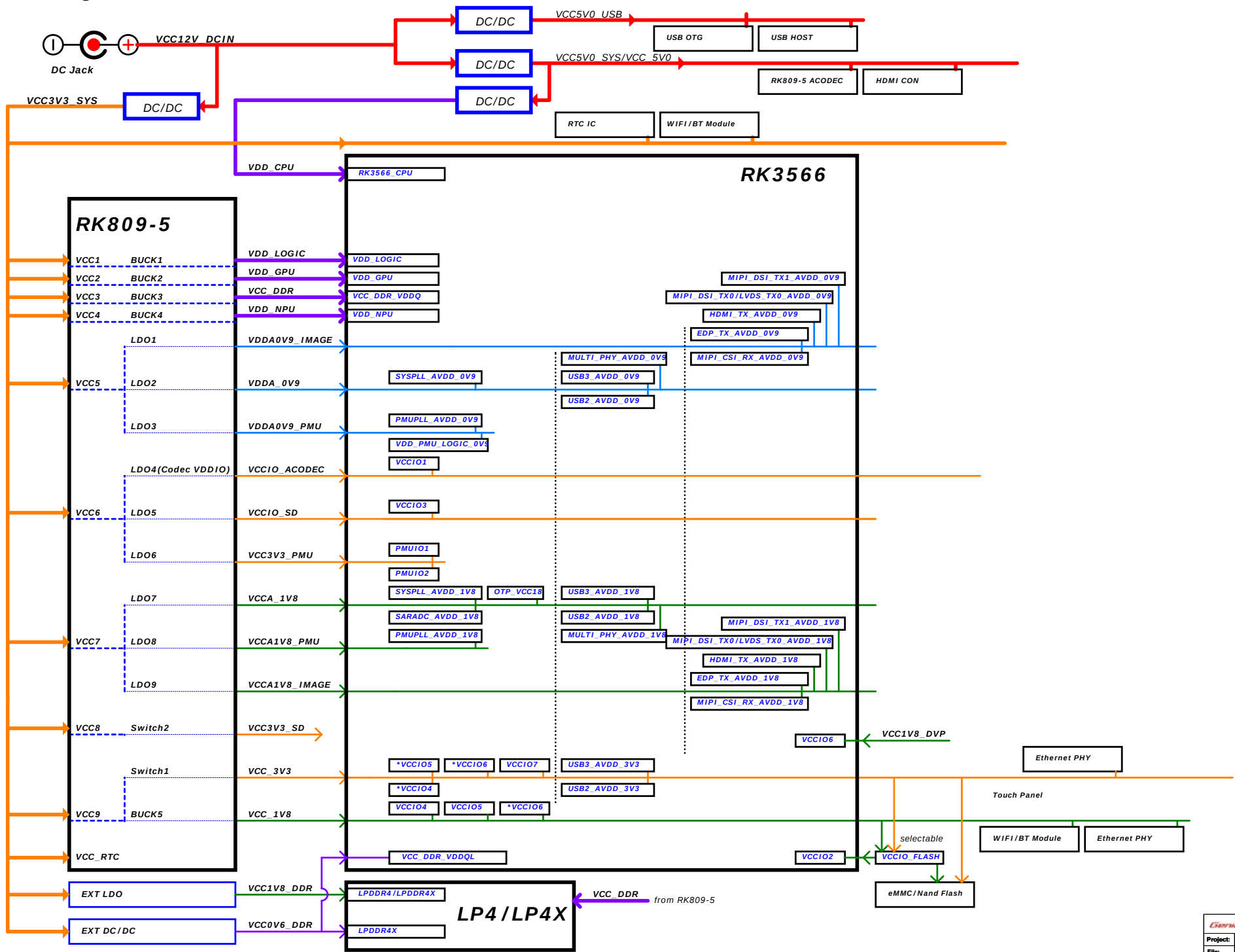


[illegible][illegible]

RK3566 Ref Block Diagram
(Typical Application Case)

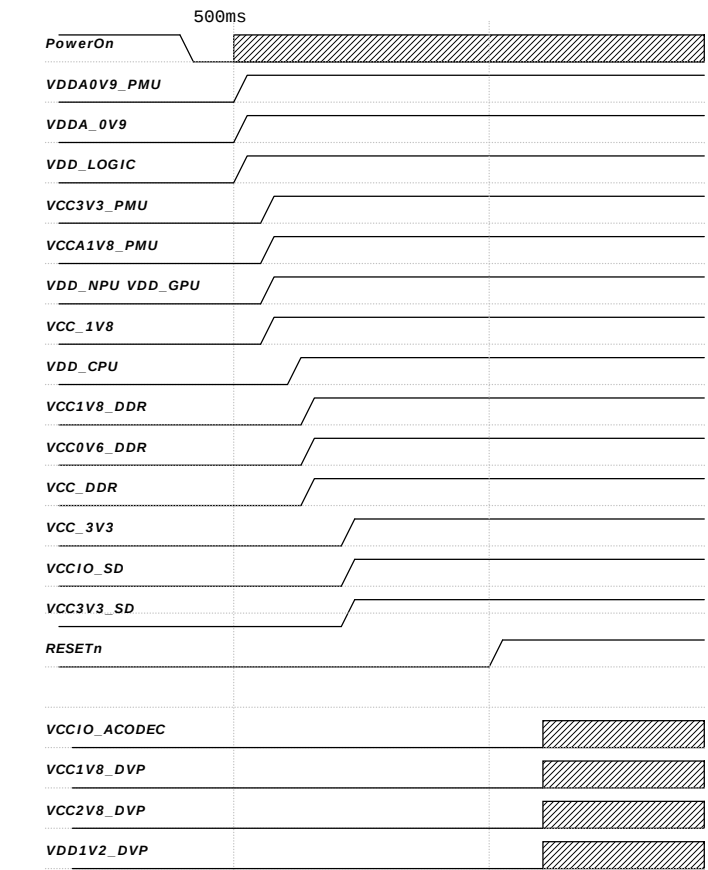


Power Diagram



Power Sequence

&Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF
VCC_SYS	EXT BUCK	2A	VDD1V2_DVP	N/A	1.2V	ON	OFF

IO Power Domain Map

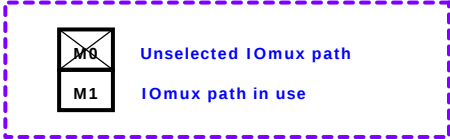
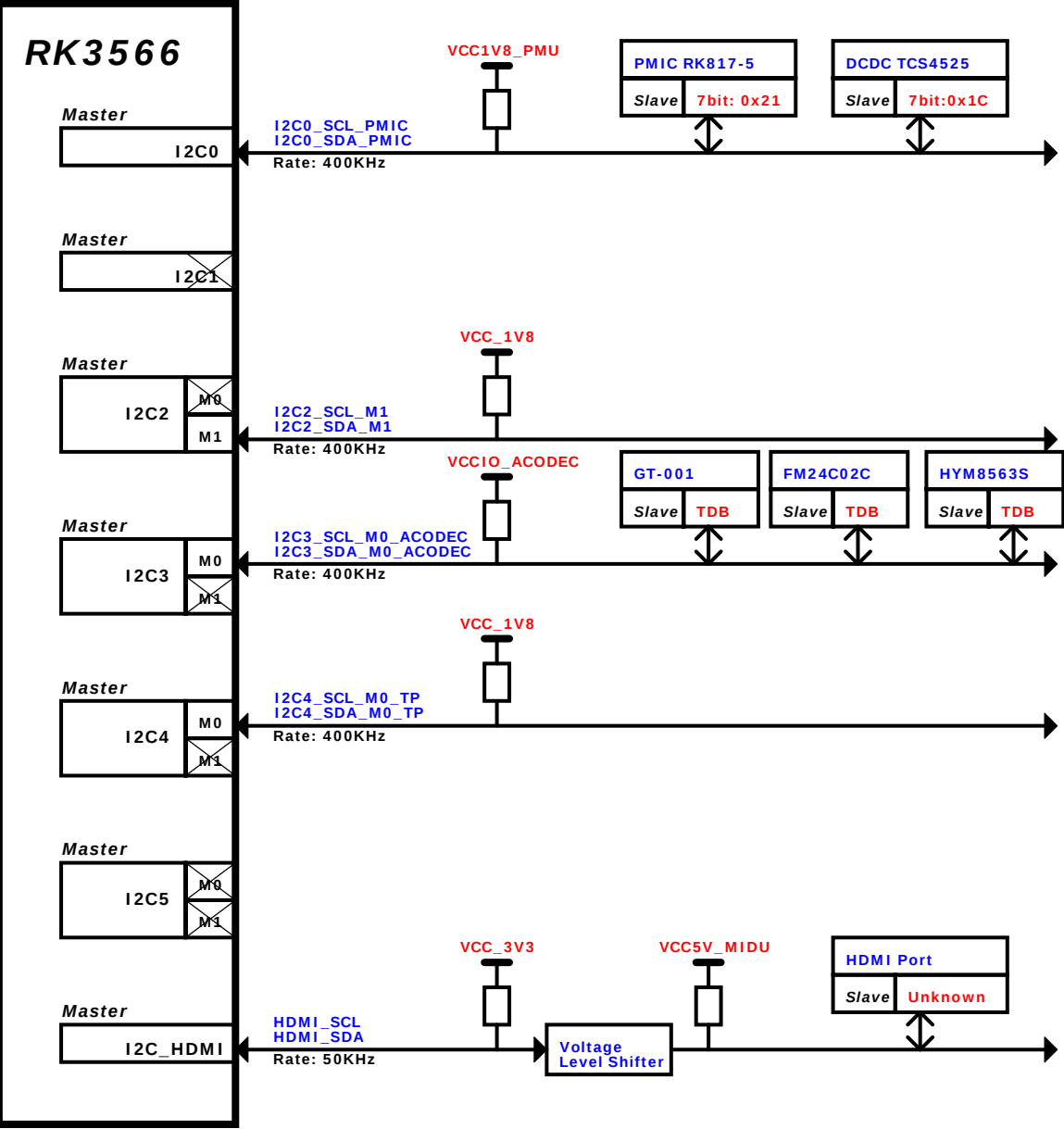
Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage		Voltage	Notes
		3.3V	1.8V	Supply Power Net Name	Power Source		
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCCA1V8_PMU	VCCA1V8_PMU	1.8V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC_1V8	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

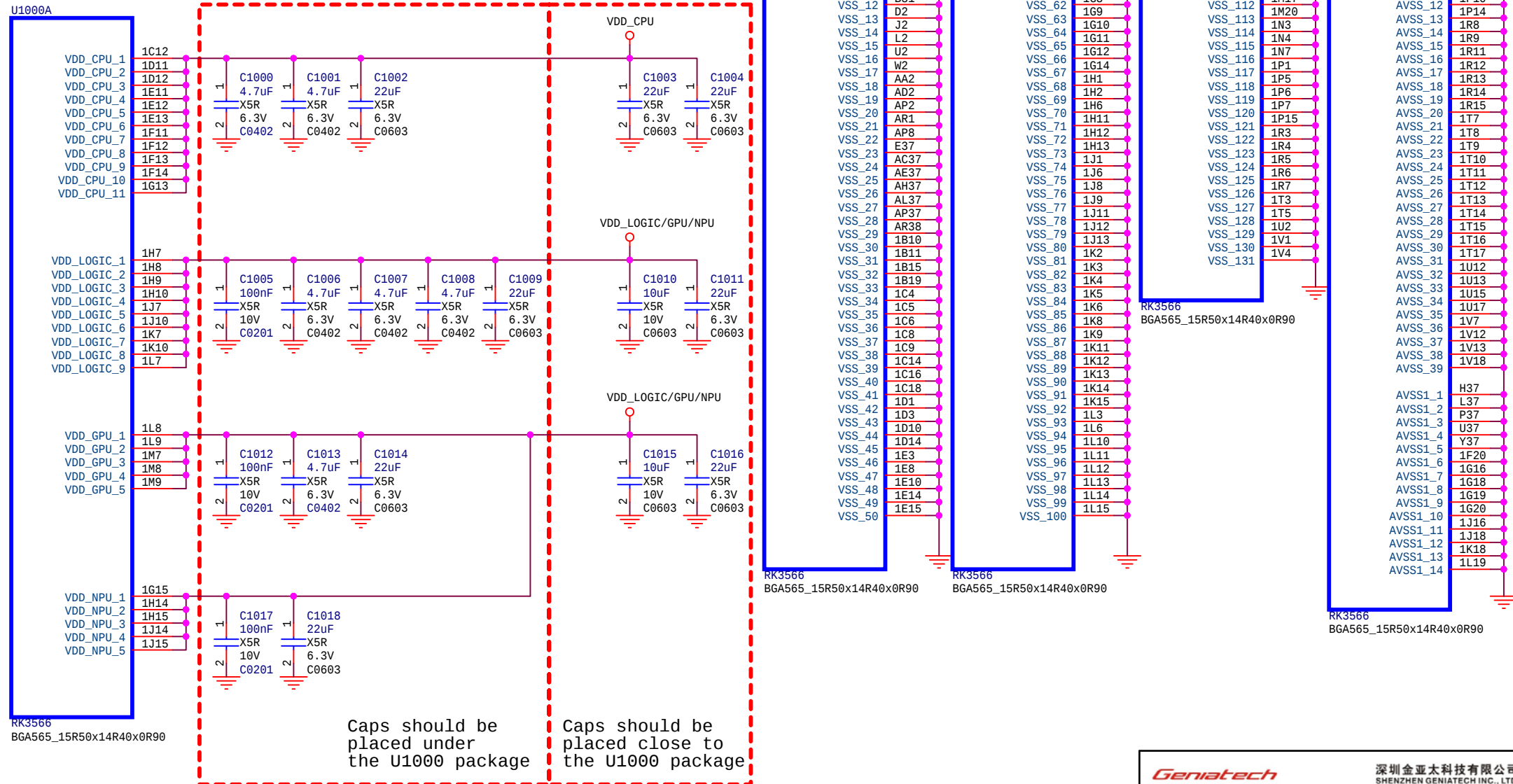
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

!!! Attention

I2C MAP



RK3566_ABCDE (Power&GND)



RK3566_F (DDR PHY)

U1000F

	DDR4	LPDDR4	DDR3	LPDDR3	DDR4	LPDDR4	DDR3	LPDDR3
DOR_D00_A	G3	DOR_D00_A / D004 D00_0_A	LPDDR4 D00_A	D003 D00 / LPDDR3 D00_0	DOR4_A0	LPDDR4 CLKP_B	D003 A0	AC9
DOR_D01_A	F2	DOR_D01_A / D004 D00_1_A	LPDDR4 D01_A	D003 D01 / LPDDR3 D00_1	DOR4_A1	LPDDR4 CLKP_A	D003 A1	AC10
DOR_D02_A	F1	DOR_D02_A / D004 D00_2_A	LPDDR4 D02_A	D003 D02 / LPDDR3 D00_2	DOR4_A2	LPDDR4 CLKP_A	D003 A2	AC11
DOR_D03_A	E5	DOR_D03_A / D004 D00_3_A	LPDDR4 D03_A	D003 D03 / LPDDR3 D00_3	DOR4_A3	LPDDR4 CLKP_A	D003 A3	AC12
DOR_D04_A	M2	DOR_D04_A / D004 D00_4_A	LPDDR4 D04_A	D003 D04 / LPDDR3 D00_4	DOR4_A4	LPDDR4 CLKP_A	D003 A4	AC13
DOR_D05_A	K3	DOR_D05_A / D004 D00_5_A	LPDDR4 D05_A	D003 D05 / LPDDR3 D00_5	DOR4_A5	LPDDR4 CLKP_A	D003 A5	AC14
DOR_D06_A	K2	DOR_D06_A / D004 D00_6_A	LPDDR4 D06_A	D003 D06 / LPDDR3 D00_6	DOR4_A6	LPDDR4 CLKP_A	D003 A6	AC15
DOR_D07_A	A2	DOR_D07_A / D004 D00_7_A	LPDDR4 D07_A	D003 D07 / LPDDR3 D00_7	DOR4_A7	LPDDR4 CLKP_A	D003 A7	AC16
DOR_D08_A	1E2	DOR_D08_A / D004 D00_8_A	LPDDR4 D08_A	D003 D08 / LPDDR3 D00_8	DOR4_A8	LPDDR4 CLKP_A	D003 A8	AC17
DOR_D09_A	R3	DOR_D09_A / D004 D00_9_A	LPDDR4 D09_A	D003 D09 / LPDDR3 D00_9	DOR4_A9	LPDDR4 CLKP_A	D003 A9	AC18
DOR_D0A_A	R2	DOR_D0A_A / D004 D00_10_A	LPDDR4 D0A_A	D003 D0A / LPDDR3 D00_10	DOR4_A10	LPDDR4 CLKP_A	D003 A10	AC19
DOR_D0B_A	R1	DOR_D0B_A / D004 D00_11_A	LPDDR4 D0B_A	D003 D0B / LPDDR3 D00_11	DOR4_A11	LPDDR4 CLKP_A	D003 A11	AC20
DOR_D0C_A	1E1	DOR_D0C_A / D004 D00_12_A	LPDDR4 D0C_A	D003 D0C / LPDDR3 D00_12	DOR4_A12	LPDDR4 CLKP_A	D003 A12	AC21
DOR_D0D_A	M1	DOR_D0D_A / D004 D00_13_A	LPDDR4 D0D_A	D003 D0D / LPDDR3 D00_13	DOR4_A13	LPDDR4 CLKP_A	D003 A13	AC22
DOR_D0E_A	1F1	DOR_D0E_A / D004 D00_14_A	LPDDR4 D0E_A	D003 D0E / LPDDR3 D00_14	DOR4_A14	LPDDR4 CLKP_A	D003 A14	AC23
DOR_D0F_A	1E0	DOR_D0F_A / D004 D00_15_A	LPDDR4 D0F_A	D003 D0F / LPDDR3 D00_15	DOR4_A15	LPDDR4 CLKP_A	D003 A15	AC24
DOR_D0G_A	1D1	DOR_D0G_A / D004 D00_16_A	LPDDR4 D0G_A	D003 D0G / LPDDR3 D00_16	DOR4_A16	LPDDR4 CLKP_A	D003 A16	AC25
DOR_D0H_A	1D0	DOR_D0H_A / D004 D00_17_A	LPDDR4 D0H_A	D003 D0H / LPDDR3 D00_17	DOR4_A17	LPDDR4 CLKP_A	D003 A17	AC26
DOR_D0I_A	1C1	DOR_D0I_A / D004 D00_18_A	LPDDR4 D0I_A	D003 D0I / LPDDR3 D00_18	DOR4_A18	LPDDR4 CLKP_A	D003 A18	AC27
DOR_D0J_A	1C0	DOR_D0J_A / D004 D00_19_A	LPDDR4 D0J_A	D003 D0J / LPDDR3 D00_19	DOR4_A19	LPDDR4 CLKP_A	D003 A19	AC28
DOR_D0K_A	1B1	DOR_D0K_A / D004 D00_20_A	LPDDR4 D0K_A	D003 D0K / LPDDR3 D00_20	DOR4_A20	LPDDR4 CLKP_A	D003 A20	AC29
DOR_D0L_A	1B0	DOR_D0L_A / D004 D00_21_A	LPDDR4 D0L_A	D003 D0L / LPDDR3 D00_21	DOR4_A21	LPDDR4 CLKP_A	D003 A21	AC30
DOR_D0M_A	1A1	DOR_D0M_A / D004 D00_22_A	LPDDR4 D0M_A	D003 D0M / LPDDR3 D00_22	DOR4_A22	LPDDR4 CLKP_A	D003 A22	AC31
DOR_D0N_A	1A0	DOR_D0N_A / D004 D00_23_A	LPDDR4 D0N_A	D003 D0N / LPDDR3 D00_23	DOR4_A23	LPDDR4 CLKP_A	D003 A23	AC32
DOR_D0O_A	191	DOR_D0O_A / D004 D00_24_A	LPDDR4 D0O_A	D003 D0O / LPDDR3 D00_24	DOR4_A24	LPDDR4 CLKP_A	D003 A24	AC33
DOR_D0P_A	190	DOR_D0P_A / D004 D00_25_A	LPDDR4 D0P_A	D003 D0P / LPDDR3 D00_25	DOR4_A25	LPDDR4 CLKP_A	D003 A25	AC34
DOR_D0Q_A	181	DOR_D0Q_A / D004 D00_26_A	LPDDR4 D0Q_A	D003 D0Q / LPDDR3 D00_26	DOR4_A26	LPDDR4 CLKP_A	D003 A26	AC35
DOR_D0R_A	180	DOR_D0R_A / D004 D00_27_A	LPDDR4 D0R_A	D003 D0R / LPDDR3 D00_27	DOR4_A27	LPDDR4 CLKP_A	D003 A27	AC36
DOR_D0S_A	171	DOR_D0S_A / D004 D00_28_A	LPDDR4 D0S_A	D003 D0S / LPDDR3 D00_28	DOR4_A28	LPDDR4 CLKP_A	D003 A28	AC37
DOR_D0T_A	170	DOR_D0T_A / D004 D00_29_A	LPDDR4 D0T_A	D003 D0T / LPDDR3 D00_29	DOR4_A29	LPDDR4 CLKP_A	D003 A29	AC38
DOR_D0U_A	161	DOR_D0U_A / D004 D00_30_A	LPDDR4 D0U_A	D003 D0U / LPDDR3 D00_30	DOR4_A30	LPDDR4 CLKP_A	D003 A30	AC39
DOR_D0V_A	160	DOR_D0V_A / D004 D00_31_A	LPDDR4 D0V_A	D003 D0V / LPDDR3 D00_31	DOR4_A31	LPDDR4 CLKP_A	D003 A31	AC40
DOR_D0W_A	151	DOR_D0W_A / D004 D00_32_A	LPDDR4 D0W_A	D003 D0W / LPDDR3 D00_32	DOR4_A32	LPDDR4 CLKP_A	D003 A32	AC41
DOR_D0X_A	150	DOR_D0X_A / D004 D00_33_A	LPDDR4 D0X_A	D003 D0X / LPDDR3 D00_33	DOR4_A33	LPDDR4 CLKP_A	D003 A33	AC42
DOR_D0Y_A	141	DOR_D0Y_A / D004 D00_34_A	LPDDR4 D0Y_A	D003 D0Y / LPDDR3 D00_34	DOR4_A34	LPDDR4 CLKP_A	D003 A34	AC43
DOR_D0Z_A	140	DOR_D0Z_A / D004 D00_35_A	LPDDR4 D0Z_A	D003 D0Z / LPDDR3 D00_35	DOR4_A35	LPDDR4 CLKP_A	D003 A35	AC44
DOR_D0A0_A	131	DOR_D0A0_A / D004 D00_36_A	LPDDR4 D0A0_A	D003 D0A0 / LPDDR3 D00_36	DOR4_A36	LPDDR4 CLKP_A	D003 A36	AC45
DOR_D0A1_A	130	DOR_D0A1_A / D004 D00_37_A	LPDDR4 D0A1_A	D003 D0A1 / LPDDR3 D00_37	DOR4_A37	LPDDR4 CLKP_A	D003 A37	AC46
DOR_D0A2_A	121	DOR_D0A2_A / D004 D00_38_A	LPDDR4 D0A2_A	D003 D0A2 / LPDDR3 D00_38	DOR4_A38	LPDDR4 CLKP_A	D003 A38	AC47
DOR_D0A3_A	120	DOR_D0A3_A / D004 D00_39_A	LPDDR4 D0A3_A	D003 D0A3 / LPDDR3 D00_39	DOR4_A39	LPDDR4 CLKP_A	D003 A39	AC48
DOR_D0A4_A	111	DOR_D0A4_A / D004 D00_40_A	LPDDR4 D0A4_A	D003 D0A4 / LPDDR3 D00_40	DOR4_A40	LPDDR4 CLKP_A	D003 A40	AC49
DOR_D0A5_A	110	DOR_D0A5_A / D004 D00_41_A	LPDDR4 D0A5_A	D003 D0A5 / LPDDR3 D00_41	DOR4_A41	LPDDR4 CLKP_A	D003 A41	AC50
DOR_D0A6_A	101	DOR_D0A6_A / D004 D00_42_A	LPDDR4 D0A6_A	D003 D0A6 / LPDDR3 D00_42	DOR4_A42	LPDDR4 CLKP_A	D003 A42	AC51
DOR_D0A7_A	100	DOR_D0A7_A / D004 D00_43_A	LPDDR4 D0A7_A	D003 D0A7 / LPDDR3 D00_43	DOR4_A43	LPDDR4 CLKP_A	D003 A43	AC52
DOR_D0A8_A	091	DOR_D0A8_A / D004 D00_44_A	LPDDR4 D0A8_A	D003 D0A8 / LPDDR3 D00_44	DOR4_A44	LPDDR4 CLKP_A	D003 A44	AC53
DOR_D0A9_A	090	DOR_D0A9_A / D004 D00_45_A	LPDDR4 D0A9_A	D003 D0A9 / LPDDR3 D00_45	DOR4_A45	LPDDR4 CLKP_A	D003 A45	AC54
DOR_D0AA_A	081	DOR_D0AA_A / D004 D00_46_A	LPDDR4 D0AA_A	D003 D0AA / LPDDR3 D00_46	DOR4_A46	LPDDR4 CLKP_A	D003 A46	AC55
DOR_D0AB_A	080	DOR_D0AB_A / D004 D00_47_A	LPDDR4 D0AB_A	D003 D0AB / LPDDR3 D00_47	DOR4_A47	LPDDR4 CLKP_A	D003 A47	AC56
DOR_D0AC_A	071	DOR_D0AC_A / D004 D00_48_A	LPDDR4 D0AC_A	D003 D0AC / LPDDR3 D00_48	DOR4_A48	LPDDR4 CLKP_A	D003 A48	AC57
DOR_D0AD_A	070	DOR_D0AD_A / D004 D00_49_A	LPDDR4 D0AD_A	D003 D0AD / LPDDR3 D00_49	DOR4_A49	LPDDR4 CLKP_A	D003 A49	AC58
DOR_D0AE_A	061	DOR_D0AE_A / D004 D00_50_A	LPDDR4 D0AE_A	D003 D0AE / LPDDR3 D00_50	DOR4_A50	LPDDR4 CLKP_A	D003 A50	AC59
DOR_D0AF_A	060	DOR_D0AF_A / D004 D00_51_A	LPDDR4 D0AF_A	D003 D0AF / LPDDR3 D00_51	DOR4_A51	LPDDR4 CLKP_A	D003 A51	AC60
DOR_D0AG_A	051	DOR_D0AG_A / D004 D00_52_A	LPDDR4 D0AG_A	D003 D0AG / LPDDR3 D00_52	DOR4_A52	LPDDR4 CLKP_A	D003 A52	AC61
DOR_D0AH_A	050	DOR_D0AH_A / D004 D00_53_A	LPDDR4 D0AH_A	D003 D0AH / LPDDR3 D00_53	DOR4_A53	LPDDR4 CLKP_A	D003 A53	AC62
DOR_D0AI_A	041	DOR_D0AI_A / D004 D00_54_A	LPDDR4 D0AI_A	D003 D0AI / LPDDR3 D00_54	DOR4_A54	LPDDR4 CLKP_A	D003 A54	AC63
DOR_D0AJ_A	040	DOR_D0AJ_A / D004 D00_55_A	LPDDR4 D0AJ_A	D003 D0AJ / LPDDR3 D00_55	DOR4_A55	LPDDR4 CLKP_A	D003 A55	AC64
DOR_D0AK_A	031	DOR_D0AK_A / D004 D00_56_A	LPDDR4 D0AK_A	D003 D0AK / LPDDR3 D00_56	DOR4_A56	LPDDR4 CLKP_A	D003 A56	AC65
DOR_D0AL_A	030	DOR_D0AL_A / D004 D00_57_A	LPDDR4 D0AL_A	D003 D0AL / LPDDR3 D00_57	DOR4_A57	LPDDR4 CLKP_A	D003 A57	AC66
DOR_D0AM_A	021	DOR_D0AM_A / D004 D00_58_A	LPDDR4 D0AM_A	D003 D0AM / LPDDR3 D00_58	DOR4_A58	LPDDR4 CLKP_A	D003 A58	AC67
DOR_D0AN_A	020	DOR_D0AN_A / D004 D00_59_A	LPDDR4 D0AN_A	D003 D0AN / LPDDR3 D00_59	DOR4_A59	LPDDR4 CLKP_A	D003 A59	AC68
DOR_D0AO_A	011	DOR_D0AO_A / D004 D00_60_A	LPDDR4 D0AO_A	D003 D0AO / LPDDR3 D00_60	DOR4_A60	LPDDR4 CLKP_A	D003 A60	AC69
DOR_D0AP_A	010	DOR_D0AP_A / D004 D00_61_A	LPDDR4 D0AP_A	D003 D0AP / LPDDR3 D00_61	DOR4_A61	LPDDR4 CLKP_A	D003 A61	AC70
DOR_D0AQ_A	001	DOR_D0AQ_A / D004 D00_62_A	LPDDR4 D0AQ_A	D003 D0AQ / LPDDR3 D00_62	DOR4_A62	LPDDR4 CLKP_A	D003 A62	AC71
DOR_D0AR_A	000	DOR_D0AR_A / D004 D00_63_A	LPDDR4 D0AR_A	D003 D0AR / LPDDR3 D00_63	DOR4_A63	LPDDR4 CLKP_A	D003 A63	AC72
DOR_D0AS_A	000	DOR_D0AS_A / D004 D00_64_A	LPDDR4 D0AS_A	D003 D0AS / LPDDR3 D00_64	DOR4_A64	LPDDR4 CLKP_A	D003 A64	AC73
DOR_D0AT_A	000	DOR_D0AT_A / D004 D00_65_A	LPDDR4 D0AT_A	D003 D0AT / LPDDR3 D00_65	DOR4_A65	LPDDR4 CLKP_A	D003 A65	AC74
DOR_D0AU_A	000	DOR_D0AU_A / D004 D00_66_A	LPDDR4 D0AU_A	D003 D0AU / LPDDR3 D00_66	DOR4_A66	LPDDR4 CLKP_A	D003 A66	AC75
DOR_D0AV_A	000	DOR_D0AV_A / D004 D00_67_A	LPDDR4 D0AV_A	D003 D0AV / LPDDR3 D00_67	DOR4_A67	LPDDR4 CLKP_A	D003 A67	AC76
DOR_D0AW_A	000	DOR_D0AW_A / D004 D00_68_A	LPDDR4 D0AW_A	D003 D0AW / LPDDR3 D00_68	DOR4_A68	LPDDR4 CLKP_A	D003 A68	AC77
DOR_D0AX_A	000	DOR_D0AX_A / D004 D00_69_A	LPDDR4 D0AX_A	D003 D0AX / LPDDR3 D00_69	DOR4_A69	LPDDR4 CLKP_A	D003 A69	AC78
DOR_D0AY_A	000	DOR_D0AY_A / D004 D00_70_A	LPDDR4 D0AY_A	D003 D0AY / LPDDR3 D00_70	DOR4_A70	LPDDR4 CLKP_A	D003 A70	AC79
DOR_D0AZ_A	000	DOR_D0AZ_A / D004 D00_71_A	LPDDR4 D0AZ_A	D003 D0AZ / LPDDR3 D00_71	DOR4_A71	LPDDR4 CLKP_A	D003 A71	AC80
DOR_D0BA_A	000	DOR_D0BA_A / D004 D00_72_A	LPDDR4 D0BA_A	D003 D0BA / LPDDR3 D00_72	DOR4_A72	LPDDR4 CLKP_A	D003 A72	AC81
DOR_D0BB_A	000	DOR_D0BB_A / D004 D00_73_A	LPDDR4 D0BB_A	D003 D0BB / LPDDR3 D00_73	DOR4_A73	LPDDR4 CLKP_A	D003 A73	AC82
DOR_D0BC_A	000	DOR_D0BC_A / D004 D00_74_A	LPDDR4 D0BC_A	D003 D0BC / LPDDR3 D00_74	DOR4_A74	LPDDR4 CLKP_A	D003 A74	AC83
DOR_D0BD_A	000	DOR_D0BD_A / D004 D00_75_A	LPDDR4 D0BD_A	D003 D0BD / LPDDR3 D00_75	DOR4_A75	LPDDR4 CLKP_A	D003 A75	AC84
DOR_D0BE_A	000	DOR_D0BE_A / D004 D00_76_A	LPDDR4 D0BE_A	D003 D0BE / LPDDR3 D00_76	DOR4_A76	LPDDR4 CLKP_A	D003 A76	AC85
DOR_D0BF_A	000	DOR_D0BF_A / D004 D00_77_A	LPDDR4 D0BF_A	D003 D0BF / LPDDR3 D00_77	DOR4_A77	LPDDR4 CLKP_A	D003 A77	AC86
DOR_D0BG_A	000	DOR_D0BG_A / D004 D00_78_A	LPDDR4 D0BG_A	D003 D0BG / LPDDR3 D00_78	DOR4_A78	LPDDR4 CLKP_A	D003 A78	AC87
DOR_D0BH_A	000	DOR_D0BH_A / D004 D00_79_A	LPDDR4 D0BH_A	D003 D0BH / LPDDR3 D00_79	DOR4_A79	LPDDR4 CLKP_A	D003 A79	AC88
DOR_D0BI_A	000	DOR_D0BI_A / D004 D00_80_A	LPDDR4 D0BI_A	D003 D0BI / LPDDR3 D00_80	DOR4_A80	LPDDR4 CLKP_A	D003 A80	AC89
DOR_D0BJ_A	000	DOR_D0BJ_A / D004 D00_81_A	LPDDR4 D0BJ_A	D003 D0BJ / LPDDR3 D00_81	DOR4_A81	LPDDR4 CLKP_A	D003 A81	AC90
DOR_D0BK_A	000	DOR_D0BK_A / D004 D00_82_A	LPDDR4 D0BK_A	D003 D0BK / LPDDR3 D00_82	DOR4_A82	LPDDR4 CLKP_A	D003 A82	AC91
DOR_D0BL_A	000	DOR_D0BL_A / D004 D00_83_A	LPDDR4 D0BL_A	D003 D0BL / LPDDR3 D00_83	DOR4_A83	LPDDR4 CLKP_A	D003 A83	AC92
DOR_D0BM_A	000	DOR_D0BM_A / D004 D00_84_A	LPDDR4 D0BM_A	D003 D0BM / LPDDR3 D00_84	DOR4_A84	LPDDR4 CLKP_A	D003 A84	AC93
DOR_D0BN_A	000	DOR_D0BN_A / D004 D00_85_A	LPDDR4 D0BN_A	D003 D0BN / LPDDR3 D00_85	DOR4_A85	LPDDR4 CLKP_A	D003 A85	AC94
DOR_D0BO_A	000	DOR_D0BO_A / D004 D00_86_A	LPDDR4 D0BO_A	D003 D0BO / LPDDR3 D00_86	DOR4_A86	LPDDR4 CLKP_A	D003 A86	AC95
DOR_D0BP_A	000	DOR_D0BP_A / D004 D00_87_A	LPDDR4 D0BP_A	D003 D0BP / LPDDR3 D00_87	DOR4_A87	LPDDR4 CLKP_A	D003 A87	AC96
DOR_D0BQ_A	000	DOR_D0BQ_A / D004 D00_88_A	LPDDR4 D0BQ_A	D003 D0BQ / LPDDR3 D00_88	DOR4_A88	LPDDR4 CLKP_A	D003 A88	AC97
DOR_D0BR_A	000	DOR_D0BR_A / D004 D00_89_A	LPDDR4 D0BR_A	D003 D0BR / LPDDR3 D00_89	DOR4_A89	LPDDR4 CLKP_A	D003 A89	AC98
DOR_D0BS_A	000	DOR_D0BS_A / D004 D00_90_A	LPDDR4 D0BS_A	D003 D0BS / LPDDR3 D00_90	DOR4_A90	LPDDR4 CLKP_A	D003 A90	AC99
DOR_D0BT_A	000	DOR_D0BT_A / D004 D00_91_A	LPDDR4 D0BT_A	D003 D0BT / LPDDR3 D00_91	DOR4_A91	LPDDR4 CLKP_A	D003 A91	AC100
DOR_D0BU_A	000	DOR_D0BU_A / D004 D00_92_A	LPDDR4 D0BU_A	D003 D0BU / LPDDR3 D00_92	DOR4_A92	LPDDR4 CLKP_A	D003 A92	AC101
DOR_D0BV_A	000	DOR_D0BV_A / D004 D00_93_A	LPDDR4 D0BV_A	D003 D0BV / LPDDR3 D00_93	DOR4_A93	LPDDR4 CLKP_A	D003 A93	AC102
DOR_D0BW_A	000	DOR_D0BW_A / D004 D00_94_A	LPDDR4 D0BW_A	D003 D0BW / LPDDR3 D00_94	DOR4_A94	LPDDR4 CLKP_A	D003 A94	AC103
DOR_D0BX_A	000	DOR_D0BX_A / D004 D00_95_A	LPDDR4 D0BX_A	D003 D0BX / LPDDR3 D00_95	DOR4_A95	LPDDR4 CLKP_A	D003 A95	AC104
DOR_D0BY_A	000	DOR_D0BY_A / D004 D00_96_A	LPDDR4 D0BY_A	D003 D0BY / LPDDR3 D00_96	DOR4_A96	LPDDR4 CLKP_A	D003 A96	AC105
DOR_D0BZ_A	000	DOR_D0BZ_A / D004 D00_97_A	LPDDR4 D0BZ_A	D003 D0BZ / LPDDR3 D00_97	DOR4_A97	LPDDR4 CLKP_A	D003 A97	AC106
DOR_D0CA_A	000	DOR_D0CA_A / D004 D00_98_A	LPDDR4 D0CA_A	D003 D0CA / LPDDR3 D00_98	DOR4_A98	LPDDR4 CLKP_A	D003 A98	AC107
DOR_D0CB_A	000	DOR_D0CB_A / D004 D00_99_A	LPDDR4 D0CB_A	D003 D0CB / LPDDR3 D00_99	DOR4_A99	LPDDR4 CLKP_A	D003 A99	AC108
DOR_D0CC_A	000	DOR_D0CC_A / D004 D00_100_A	LPDDR4 D0CC_A	D003 D0CC / LPDDR3 D00_100	DOR4_A100	LPDDR4 CLKP_A	D003 A100	AC109
DOR_D0CD_A	000	DOR_D0CD_A / D004 D00_101_A	LPDDR4 D0CD_A	D003 D0CD / LPDDR3 D00_101	DOR4_A101	LPDDR4 CLKP_A	D003 A101	AC110
DOR_D0CE_A	000	DOR_D0CE_A / D004 D00_102_A	LPDDR4 D0CE_A	D003 D0CE / LPDDR3 D00_102	DOR4_A102	LPDDR4 CLKP_A	D003 A102	AC111
DOR_D0CF_A	000	DOR_D0CF_A / D004 D00_103_A	LPDDR4 D0CF_A	D003 D0CF / LPDDR3 D00_103	DOR4_A103	LPDDR4 CLKP_A	D003 A103	AC112
DOR_D0CG_A	000	DOR_D0CG_A / D004 D00_10						

RK3566_I (VCCIO2 Domain)

U1000I

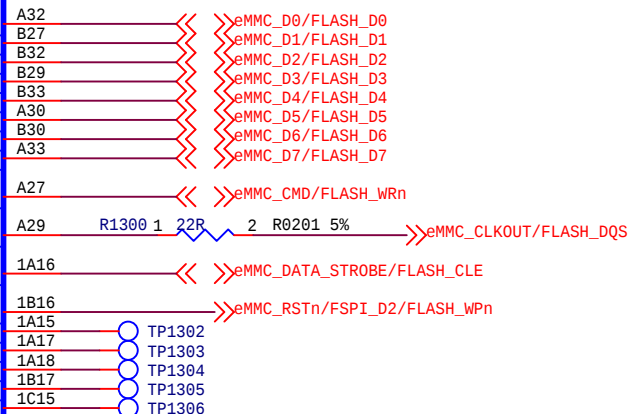
VCCIO2 Domain

Operating Voltage=1.8V/3.3V

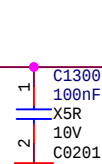
EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d
EMMC_DATA_STROBE	/ FSPI_CS1n	/ FLASH_CLE
EMMC_RSTn	/ FSPI_D2	/ FLASH_WPn
FSPI_CLK	/ FLASH_ALE	/ GPIO1_D0_d
FSPI_D0	/ FLASH_RDY	/ GPIO1_D1_u
FSPI_D1	/ FLASH_RDn	/ GPIO1_D2_u
FSPI_CS0n	/ FLASH_CS0n	/ GPIO1_D3_u
FSPI_D3	/ FLASH_CS1n	/ GPIO1_D4_u

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

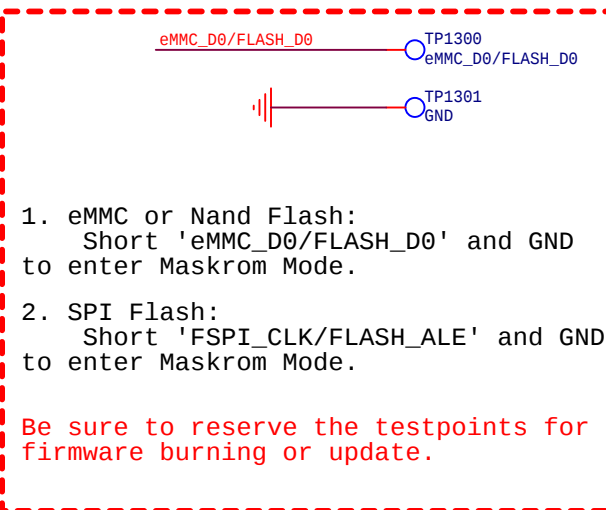
RK3566
BGA565_15R50x14R40x0R90



VCCIO2



Caps should be placed under the U1000 package



1. eMMC or Nand Flash:
Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.
2. SPI Flash:
Short 'FSPI_CLK/FLASH_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

RK3566_J (VCCIO3 Domain)

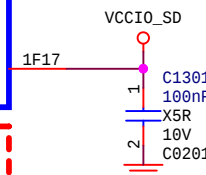
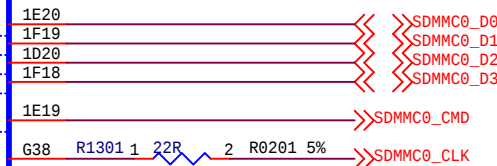
U1000J

VCCIO3 Domain

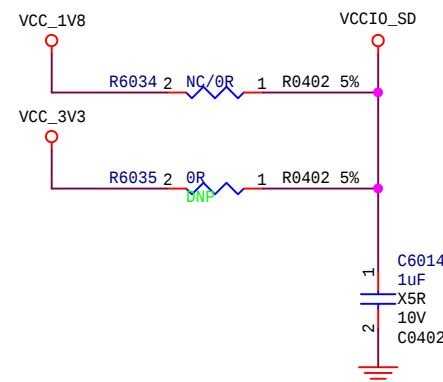
Operating Voltage=1.8V/3.3V

PWM8_M1	/ SDMMC0_D0	/ UART2_TX_M1	/ UART6_TX_M1	/ GPIO1_D5_u
PWM9_M1	/ SDMMC0_D1	/ UART2_RX_M1	/ UART6_RX_M1	/ GPIO1_D6_u
SDMMC0_D2	/ ARM_JTAG_TCK	/ UART5_CTSn_M0	/ GPIO1_D7_u	/ GPIO1_D7_u
SDMMC0_D3	/ ARM_JTAG_TMS	/ UART5_RTSn_M0	/ GPIO1_D8_u	/ GPIO1_D8_u
PWM10_M1	/ SDMMC0_CMD	/ UART5_RX_M0	/ GPIO2_A1_u	/ GPIO2_A1_u
SDMMC0_CLK	/ TEST_CLKOUT	/ UART5_TX_M0	/ GPIO2_A2_d	/ GPIO2_A2_d

RK3566
BGA565_15R50x14R40x0R90



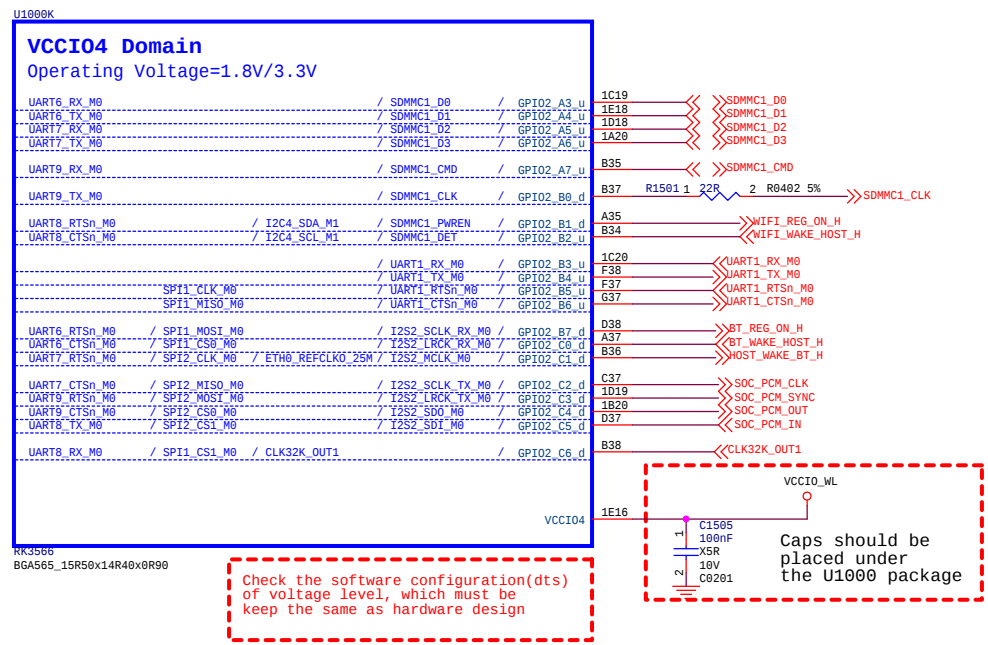
Caps should be placed under the U1000 package



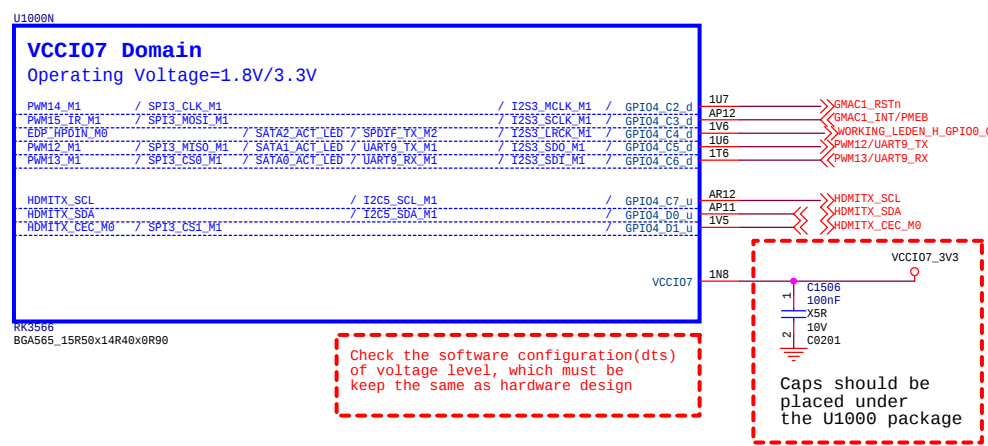
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

<i>Geniatech</i>		深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD	
Project:	RK3566_TABLET_REF		
File:	09.RK3566_FlashSDController		
Date:	Saturday, October 28, 2023		Rev: V1.0
Designed by:	wu	Reviewed by: CJX	Sheet: 9 of 27

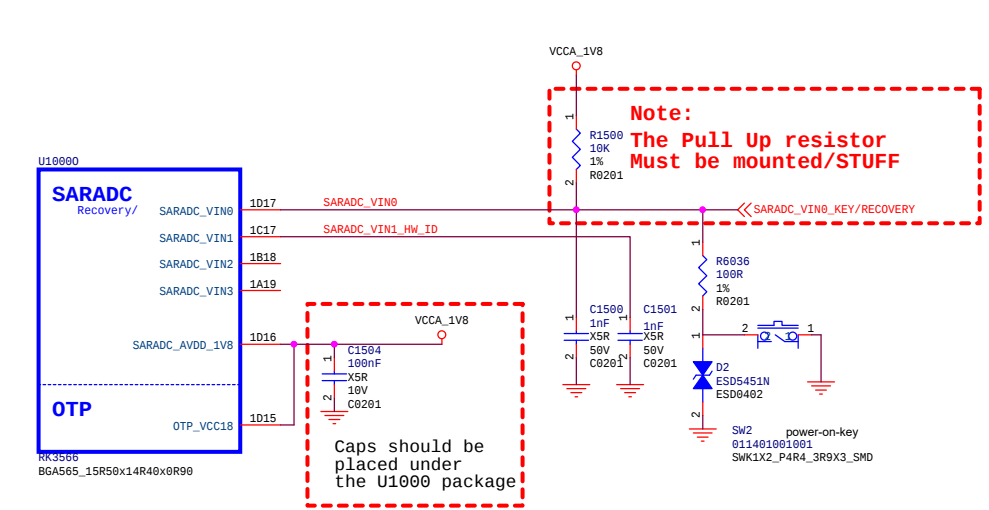
RK3566_K(VCCIO4 Domain)



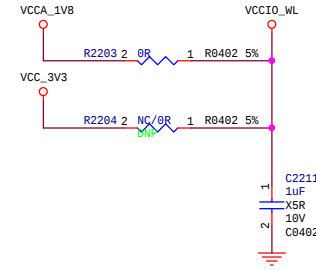
RK3566_N(VCCIO7 Domain)



RK3566_0(SARADC/OTP)

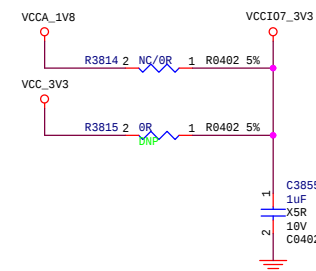
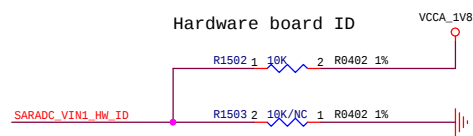


VCCIO_WL

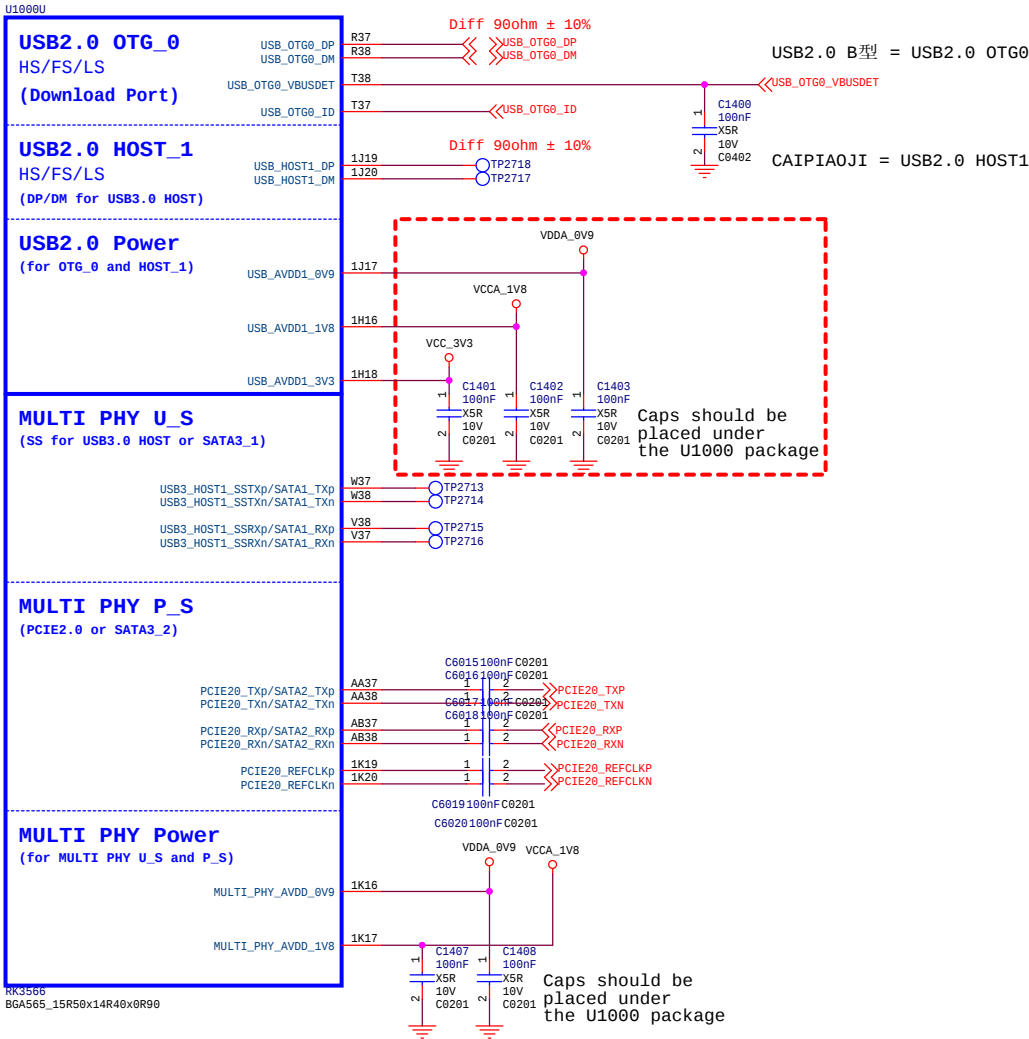


SARADC_VIN1_HW_ID	Rup	Rdown	ADC	
Version 1	10K	DNP	1023	1.8V
Version 2	20K	100K	852	1.5V
Version 3	18K	36K	681	1.2V
Version 4	51K	51K	512	0.9V
Version 5	36K	18K	340	0.6V
Version 6	100K	20K	170	0.3V
Version 7	DNP	10K	0	0V

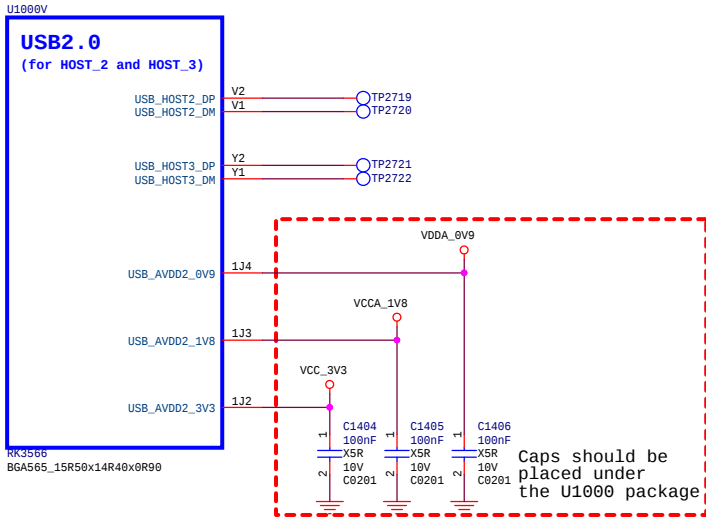
Hardware board ID



RK3566_U(USB3.0/PCIe2.0x1/SATA)



RK3566_V(USB2.0 HOST)



RK3566_P(MIPI_CSI_RX)

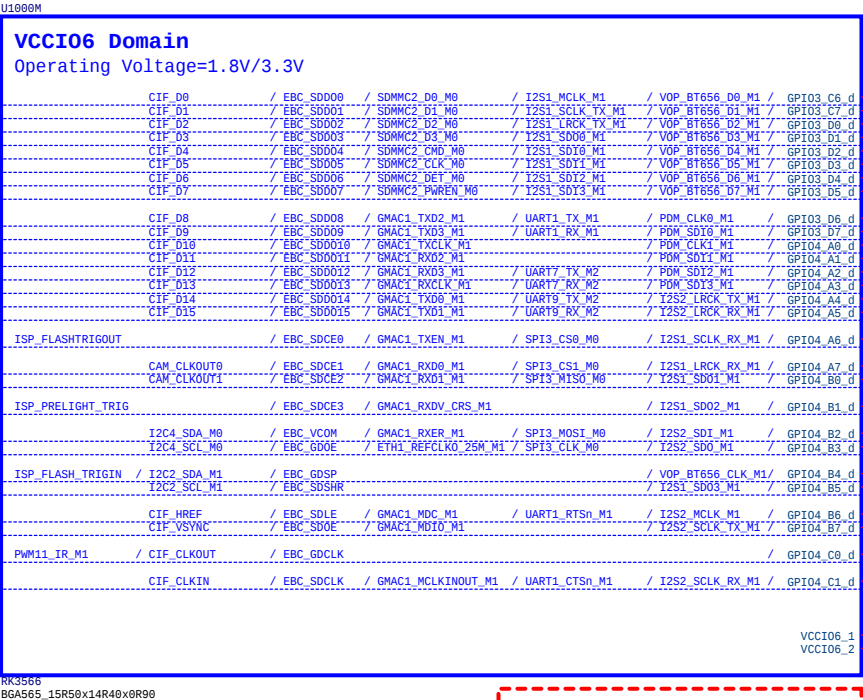
Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Usage of CIF Interface				
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

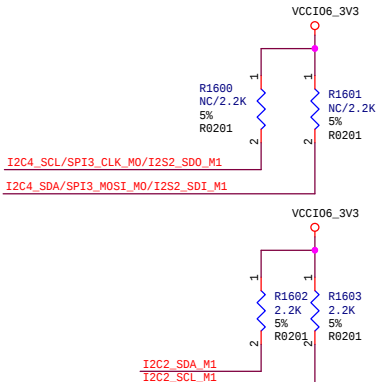
RK3566_M(VCCIO6 Domain)



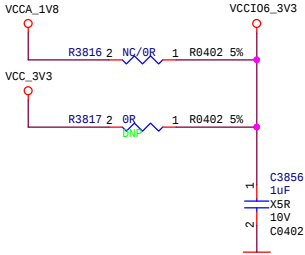
RK3566
BGA565_15R50x14R40x0R90

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Caps should be placed under the U1000 package

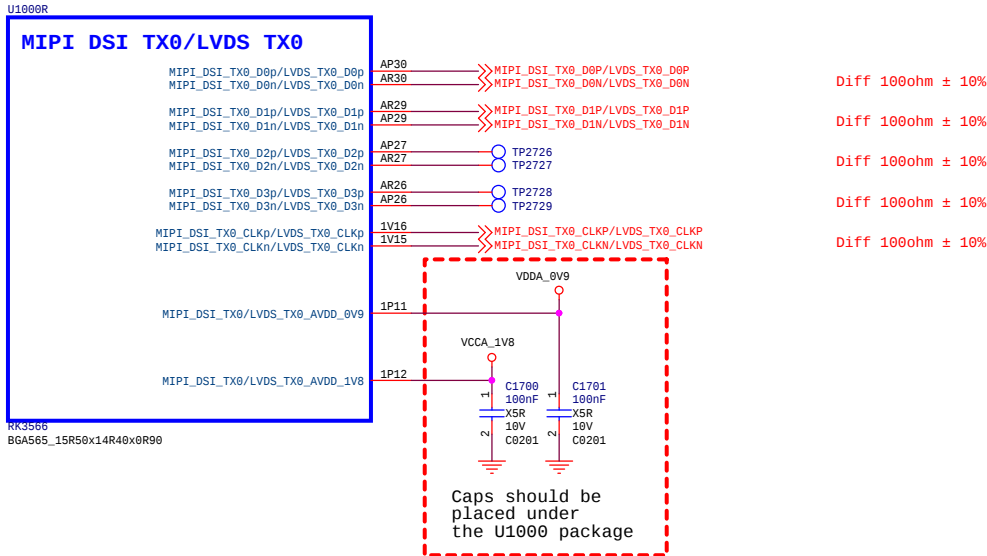


Note:
default VCCIO of Camera is 1.8V

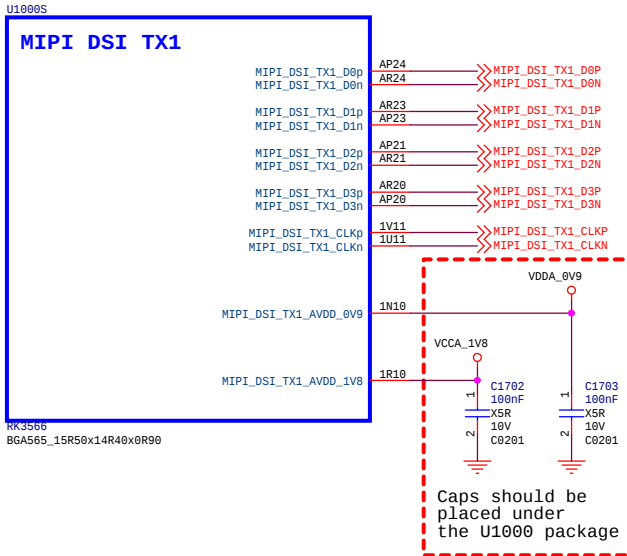


<i>Geniatech</i>		深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD	
Project:	RK3566_TABLET_REF		
File:	12.RK3566_VI_Interface		
Date:	Saturday, October 28, 2023	Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX
Sheet:	12	of	27

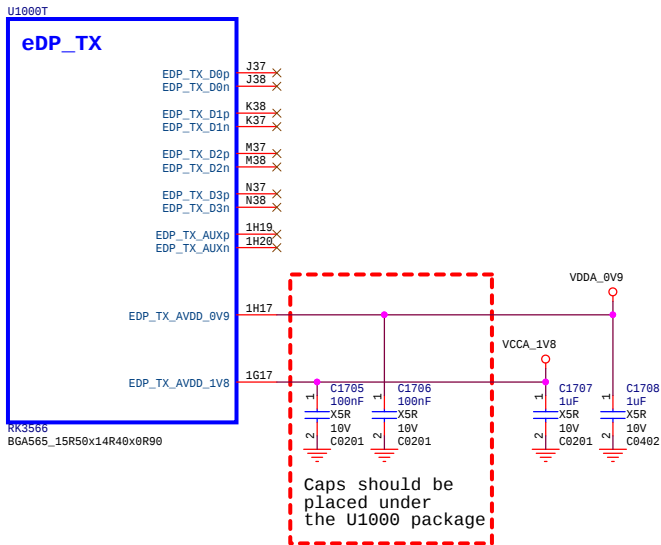
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



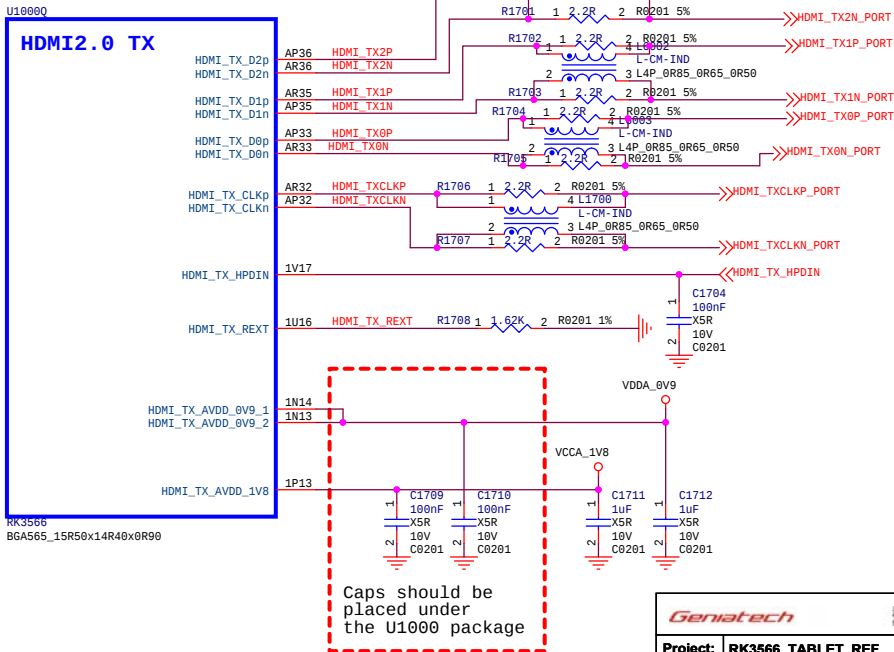
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



RK3566_L (VCCIO5 Domain)

U1000L

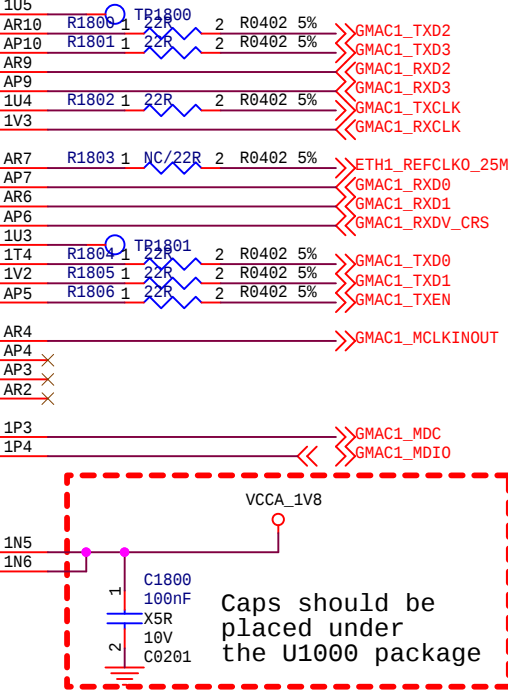
VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1		/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6	/ ETH1_REFCLK0_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0		/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0		/ GPIO3_B6_d
PWM12_M0		/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0		/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3566
BGA565_15R50x14R40x0R90

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design



RK3566_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain
Operating Voltage=1.8V/3.3V

/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u	A22	>>I2C3_SDA_ACODEC
/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u	B22	>>I2C3_SCL_ACODEC
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0	/ GPIO1_A2_d	A23	>>I2S1_MCLK_M0_PMIC
SCR_I0	/ I2S1_SCLK_TX_M0 / UART3_CTSn_M0	/ I2S1_SCLK_RX_M0 / UART4_RX_M0	/ GPIO1_A3_d	B23	>>I2S1_SCLK_TX_M0_PMIC
		/ PDM_CLK1_M0 / SPDIF_TX_M0	/ GPIO1_A4_d	1A13	PD_NS1 TP1902
SCR_RST	/ I2S1_LRCK_TX_M0 / UART4_RTSn_M0	/ I2S1_LRCK_RX_M0 / UART4_TX_M0	/ GPIO1_A5_d	B24	>>I2S1_LRCK_TX_M0_PMIC
		/ PDM_CLK0_M0 / AUDIOPWM_ROUT_p	/ GPIO1_A6_d	1A14	>>PDM_CLK0_M0_PMIC
SCR_DET	/ I2S1_SD00_M0 / UART4_CTSn_M0	/ I2S1_SD01_M0 / I2S1_SD13_M0	/ GPIO1_A7_d	B25	>>I2S1_SD00_M0_PMIC
		/ PDM_SDI3_M0 / PCIE20_CLKREQn_M2	/ GPIO1_B0_d	1B13	>>PCie_CLK_nRSQ
		/ I2S1_SD02_M0 / I2S1_SD12_M0	/ GPIO1_B1_d	A26	TP1904
		/ PDM_SDI2_M0 / PCIE20_WAKEn_M2	/ GPIO1_B2_d	B26	>>PCie_nRST
		/ I2S1_SD03_M0 / I2S1_SD11_M0	/ GPIO1_B3_d	1B14	>>I2S1_SDIO_M0/PDM_SDI0_M0_PMIC
		/ PDM_SDI1_M0 / PCIE20_PERStn_M2			
		/ I2S1_SD10_M0 / PDM_SDI0_M0			

RK3566
BGA565_15R50x14R40x0R90

VCCIO1

Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

VCC_3V3

C1900
100nF
X5R
10V
C0201

Caps should be placed under the U1000 package

VCCIO_ACODEC = 3.3V as default

I2C3_SDA_ACODEC
I2C3_SCL_ACODEC

R6044 2.2K 5%
R0201

R6045 2.2K 5%
R0201

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SHENZHEN GENIATECH INC., LTD

Project: RK3566_TABLET_REF

File: 15.RK3566_Audio_Interface

Date: Saturday, October 28, 2023 Rev: V1.0

Designed by: wu Reviewed by: CJX Sheet: 15 of 27

RK3566_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain
Operating Voltage=1.8V/3.3V

/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u	A22	>> I2C3_SDA_ACODEC
/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u	B22	>> I2C3_SCL_ACODEC
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0	/ GPIO1_A2_d	A23	>> I2S1_MCLK_M0_PMIC
SCR_I0	/ I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ GPIO1_A3_d	B23	>> I2S1_SCLK_TX_M0_PMIC
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0	1A13	PD_NS1 TP1902
SCR_RST	/ I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ GPIO1_A5_d	B24	>> I2S1_LRCK_TX_M0_PMIC
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ GPIO1_A6_d	1A14	>> PDM_CLK0_M0_PMIC
SCR_DET	/ I2S1_SD00_M0	/ UART4_CTSn_M0	/ GPIO1_A7_d	B25	>> I2S1_SD00_M0_PMIC
I2S1_SD01_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	1B13	>> PCIe_CLK_nRSQ
I2S1_SD02_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	A26	TP1904
I2S1_SD03_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2	B26	>> PCIe_nRST
I2S1_SDI0_M0	/ PDM_SDI0_M0	/ GPIO1_B3_d		1B14	>> I2S1_SDI0_M0/PDM_SDI0_M0_PMIC

RK3566
BGA565_15R50x14R40x0R90

VCCIO1

Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

VCC_3V3

Caps should be placed under the U1000 package

VCCIO_ACODEC = 3.3V as default

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SHENZHEN GENIATECH INC., LTD

Project: RK3566_TABLET_REF	
File: 15.RK3566_Audio_Interface	
Date:	Saturday, October 28, 2023
Designed by:	wu
Reviewed by:	CJX
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[illegible]

RK3566_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain
Operating Voltage=1.8V/3.3V

/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u	A22	>>I2C3_SDA_ACODEC
/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u	B22	>>I2C3_SCL_ACODEC
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0	/ GPIO1_A2_d	A23	>>I2S1_MCLK_M0_PMIC
SCR_I0	/ I2S1_SCLK_TX_M0 / UART3_CTSn_M0	/ I2S1_SCLK_RX_M0 / UART4_RX_M0	/ PDM_CLK1_M0 / SPDIF_TX_M0	GPI01_A3_d GPI01_A4_d	I2S1_SCLK_TX_M0_PMIC PD_NS1 TP1902
SCR_RST	/ I2S1_LRCK_TX_M0 / UART4_RTSn_M0	/ I2S1_LRCK_RX_M0 / UART4_TX_M0	/ PDM_CLK0_M0 / AUDIOPWM_ROUT_p	GPI01_A5_d GPI01_A6_d	I2S1_LRCK_TX_M0_PMIC PDM_CLK0_M0_PMIC
SCR_DET	/ I2S1_SD00_M0 / UART4_CTSn_M0	/ I2S1_SD01_M0 / I2S1_SD13_M0	/ PDM_SDI3_M0 / PCIE20_CLKREQn_M2	GPI01_A7_d GPI01_B0_d	I2S1_SD00_M0_PMIC PCie_CLK_nRSQ
	/ I2S1_SD02_M0 / I2S1_SD12_M0	/ PDM_SDI2_M0 / PCIE20_WAKEn_M2	/ GPI01_B1_d	A26	TP1904
	/ I2S1_SD03_M0 / I2S1_SD11_M0	/ PDM_SDI1_M0 / PCIE20_PERSTn_M2	/ GPI01_B2_d	B26	PCie_nRST
	/ I2S1_SD10_M0 / PDM_SDI0_M0	/ GPI01_B3_d	1B14	>>I2S1_SDIO_M0/PDM_SDI0_M0_PMIC	

RK3566
BGA565_15R50x14R40x0R90

VCCIO1

Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

VCC_3V3

C1900
100nF
X5R
10V
C0201

Caps should be placed under the U1000 package

VCCIO_ACODEC = 3.3V as default

VCC_3V3

R6044
2.2K
5%
R0201

R6045
2.2K
5%
R0201

I2C3_SDA_ACODEC
I2C3_SCL_ACODEC

I2S1_MCLK_M0_PMIC

I2S1_SCLK_TX_M0_PMIC

PDM_CLK0_M0_PMIC

I2S1_LRCK_TX_M0_PMIC

I2S1_SD00_M0_PMIC

PCie_CLK_nRSQ

TP1904

PCie_nRST

I2S1_SDIO_M0/PDM_SDI0_M0_PMIC

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SHENZHEN GENIATECH INC., LTD

Project: RK3566_TABLET_REF	
File: 15.RK3566_Audio_Interface	
Date:	Saturday, October 28, 2023
Designed by:	wu
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[illegible]

RK3566_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain
Operating Voltage=1.8V/3.3V

/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u	A22	>>I2C3_SDA_ACODEC
/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u	B22	>>I2C3_SCL_ACODEC
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0	/ GPIO1_A2_d	A23	>>I2S1_MCLK_M0_PMIC
SCR_I0	/ I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ GPIO1_A3_d	B23	>>I2S1_SCLK_TX_M0_PMIC
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0	1A13	PD_NS1 TP1902
SCR_RST	/ I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ GPIO1_A5_d	B24	>>I2S1_LRCK_TX_M0_PMIC
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ GPIO1_A6_d	1A14	>>PDM_CLK0_M0_PMIC
SCR_DET	/ I2S1_SD00_M0	/ UART4_CTSn_M0	/ GPIO1_A7_d	B25	>>I2S1_SD00_M0_PMIC
I2S1_SD01_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	1B13	>>PCie_CLK_nRSQ
I2S1_SD02_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	A26	TP1904
I2S1_SD03_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2	B26	>>PCie_nRST
I2S1_SDI0_M0	/ PDM_SDI0_M0	/ GPIO1_B3_d		1B14	>>I2S1_SDI0_M0/PDM_SDI0_M0_PMIC

RK3566
BGA565_15R50x14R40x0R90

VCCIO1

Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

VCC_3V3

Caps should be placed under the U1000 package

VCCIO_ACODEC = 3.3V as default

Geniatech 深圳金亚太科技有限公司
SHENZHEN GENIATECH INC., LTD

Project: RK3566_TABLET_REF	
File: 15.RK3566_Audio_Interface	
Date:	Saturday, October 28, 2023
Designed by:	wu
Reviewed by:	CJX
Rev:	V1.0
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[illegible]

RK3566_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain
Operating Voltage=1.8V/3.3V

/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u	A22	>> I2C3_SDA_ACODEC
/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u	B22	>> I2C3_SCL_ACODEC
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0	/ GPIO1_A2_d	A23	>> I2S1_MCLK_M0_PMIC
SCR_I0	/ I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ GPIO1_A3_d	B23	>> I2S1_SCLK_TX_M0_PMIC
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0	1A13	PD_NS1 TP1902
SCR_RST	/ I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ GPIO1_A5_d	B24	>> I2S1_LRCK_TX_M0_PMIC
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ GPIO1_A6_d	1A14	>> PDM_CLK0_M0_PMIC
SCR_DET	/ I2S1_SD00_M0	/ UART4_CTSn_M0	/ GPIO1_A7_d	B25	>> I2S1_SD00_M0_PMIC
I2S1_SD01_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	1B13	>> PCIe_CLK_nRSQ
I2S1_SD02_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	A26	TP1904
I2S1_SD03_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2	B26	>> PCIe_nRST
I2S1_SDI0_M0	/ PDM_SDI0_M0	/ GPIO1_B3_d		1B14	>> I2S1_SDI0_M0/PDM_SDI0_M0_PMIC

RK3566
BGA565_15R50x14R40x0R90

VCCIO1

Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design

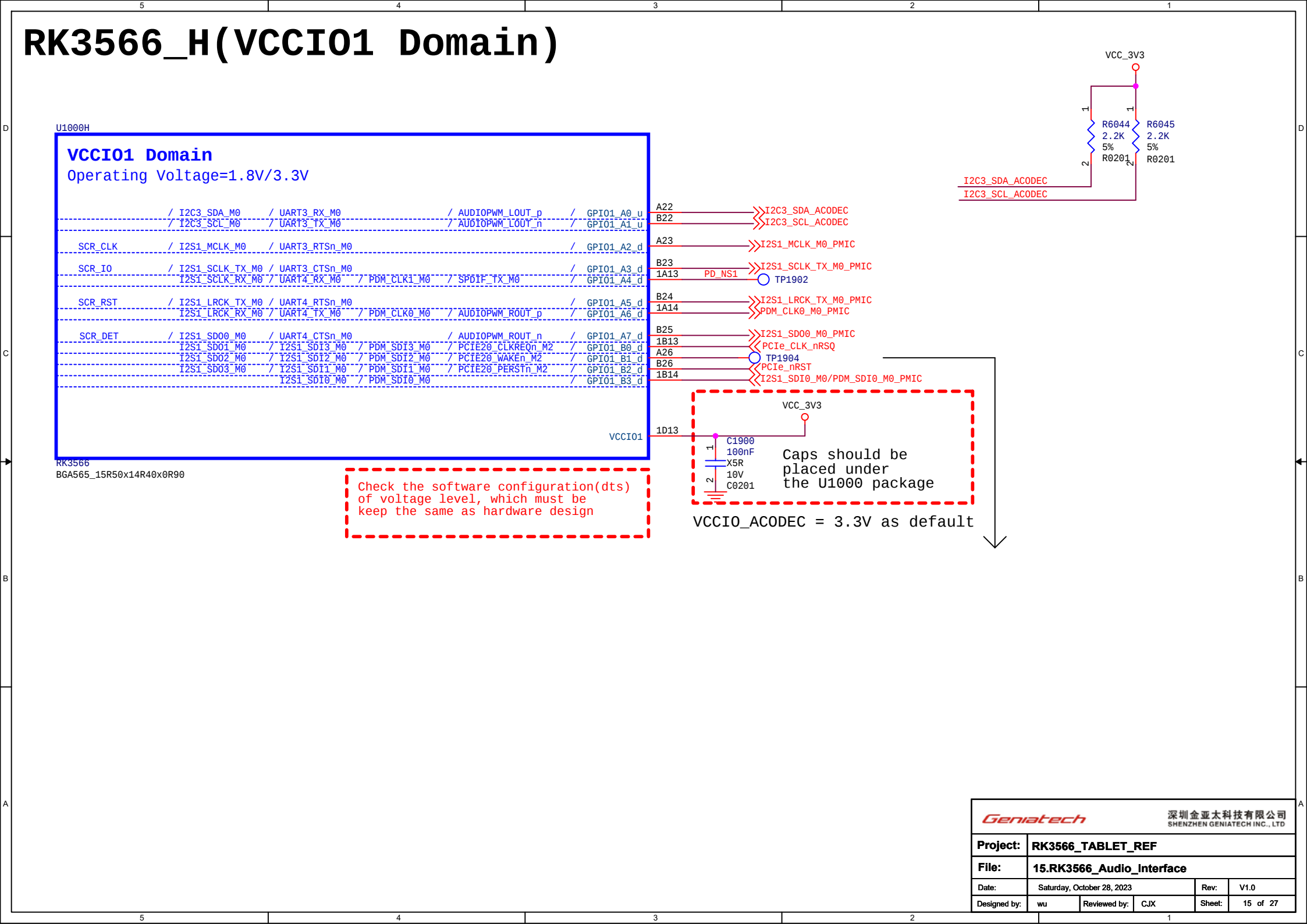
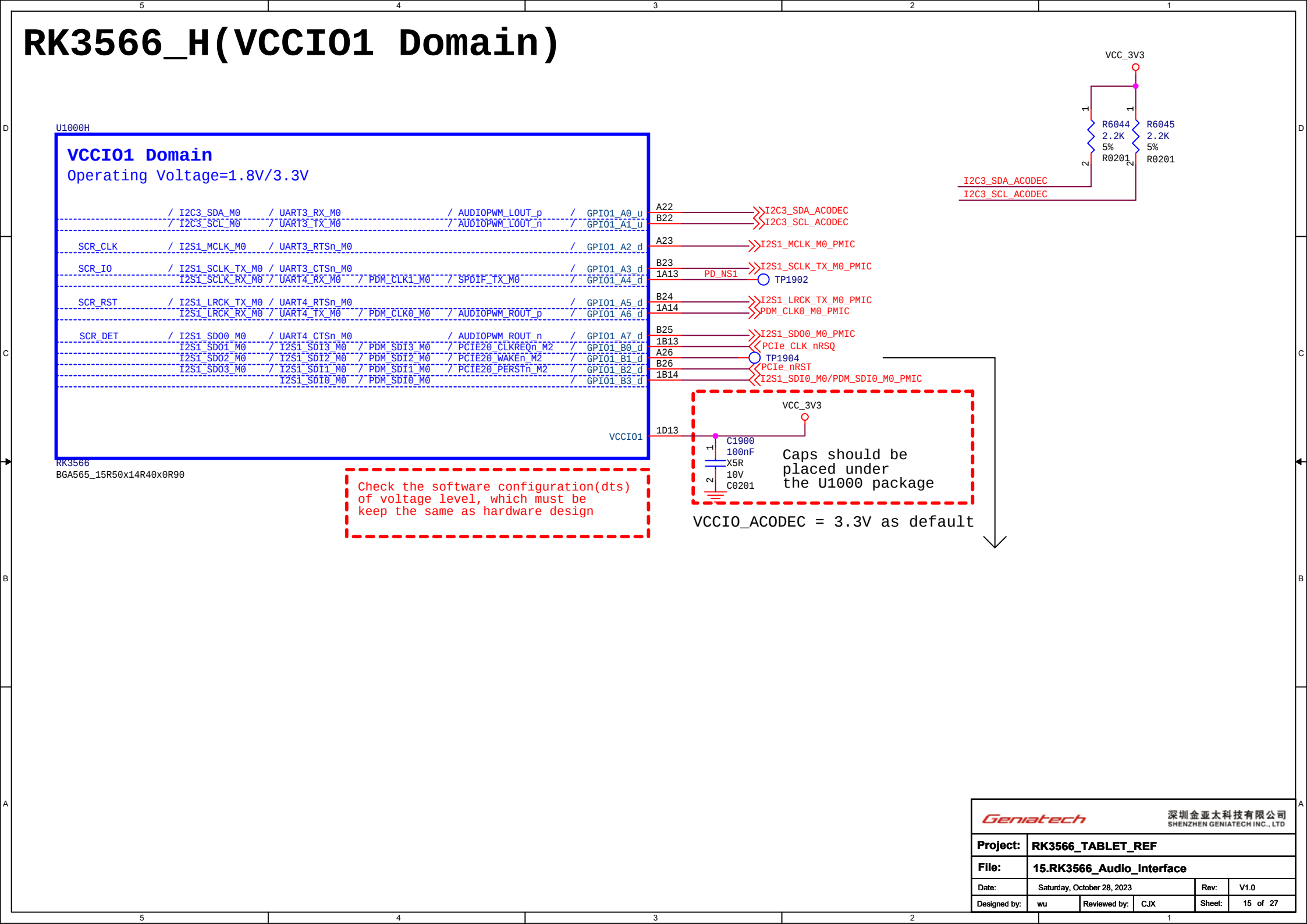
VCC_3V3

Caps should be placed under the U1000 package

VCCIO_ACODEC = 3.3V as default

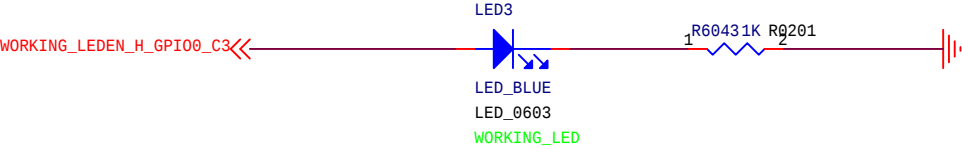
Geniatech 深圳金亚太科技有限公司
SHENZHEN GENIATECH INC., LTD

Project: RK3566_TABLET_REF	
File: 15.RK3566_Audio_Interface	
Date:	Saturday, October 28, 2023
Designed by:	wu
Reviewed by:	CJX
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Sheet:	15 of 27

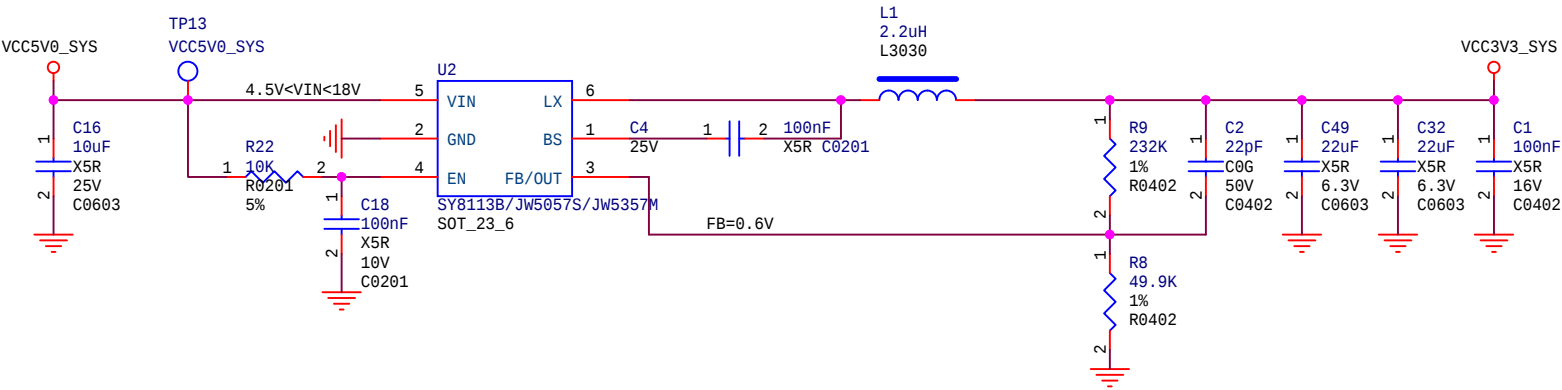
[illegible]

12V / 3A DCIN

VCC5V0_SYS



VCC3V3_SYS



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Project: RK3566_TABLET_REF

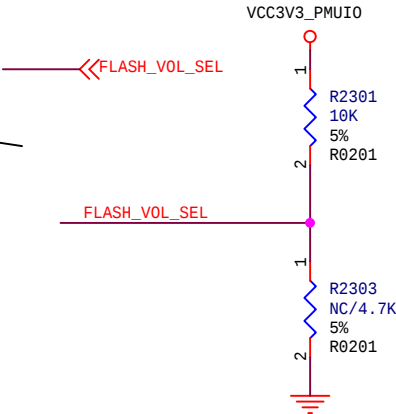
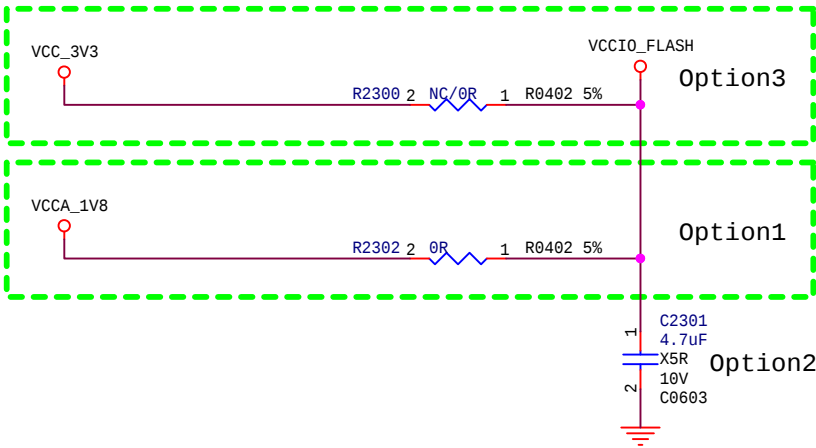
File: 16.Power_DC IN 5V

Date: Saturday, October 28, 2023 Rev: <Revision>

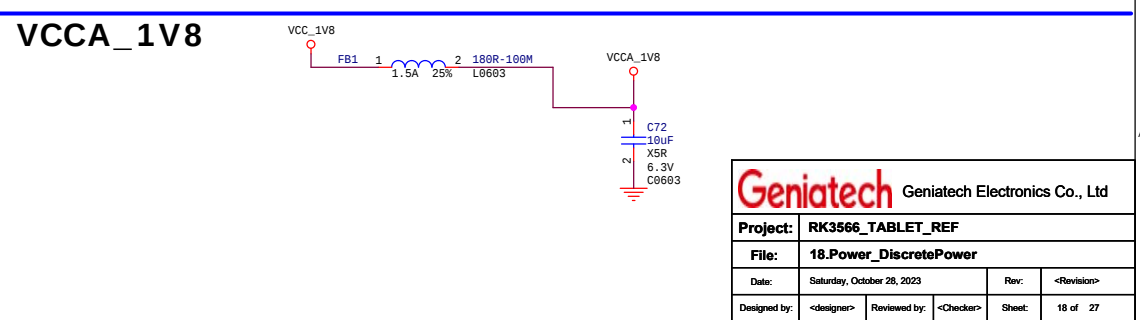
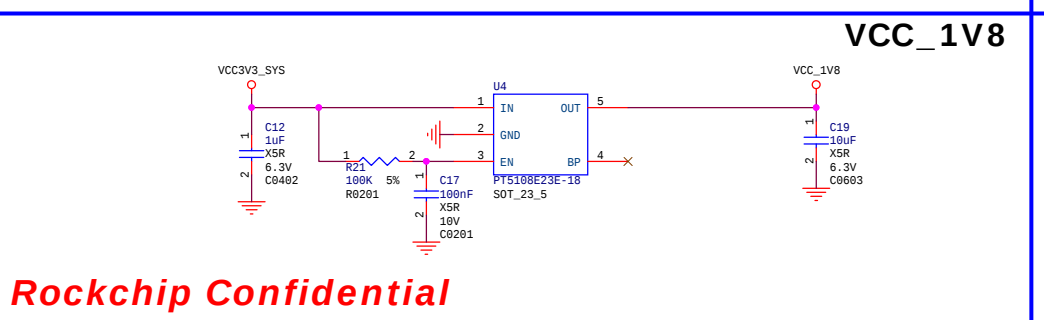
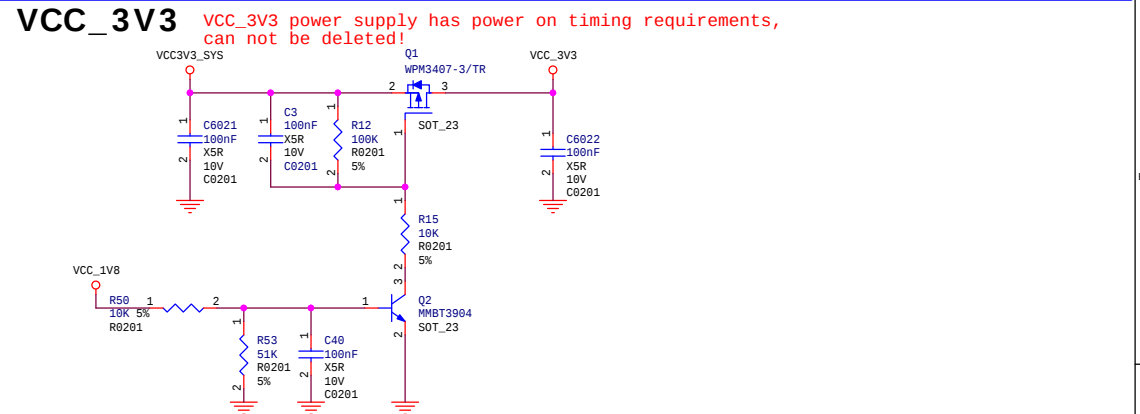
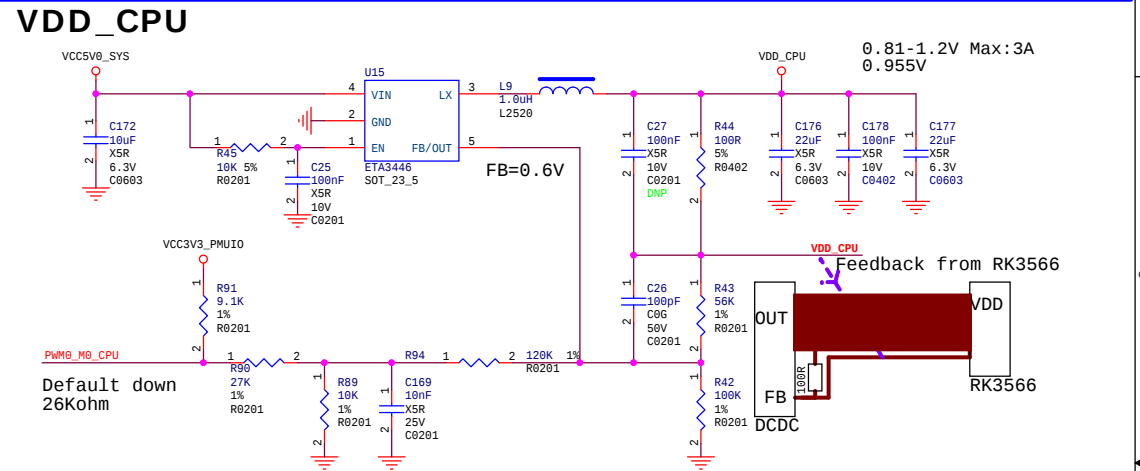
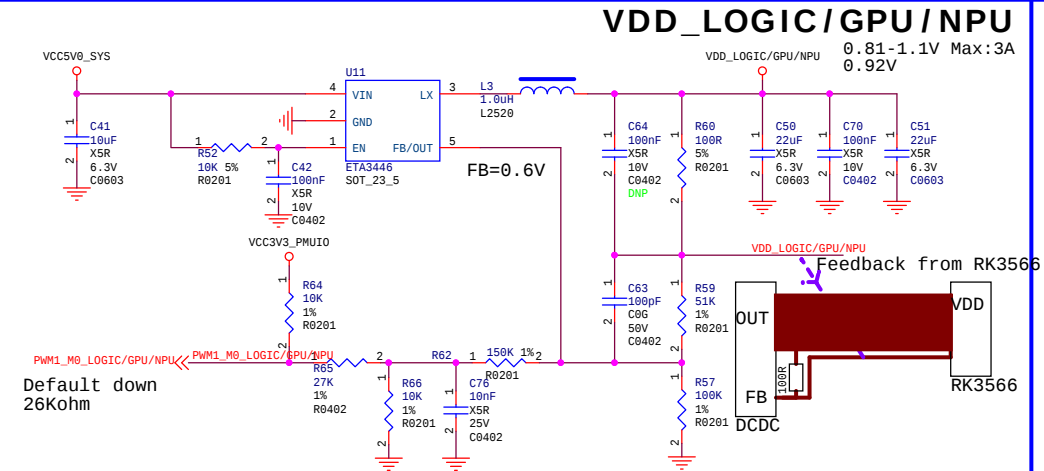
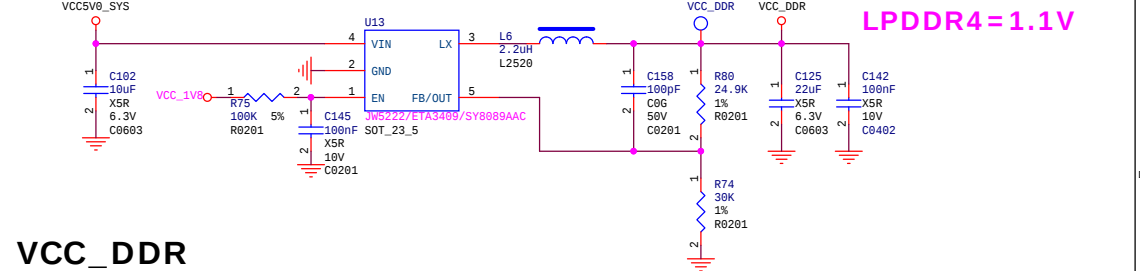
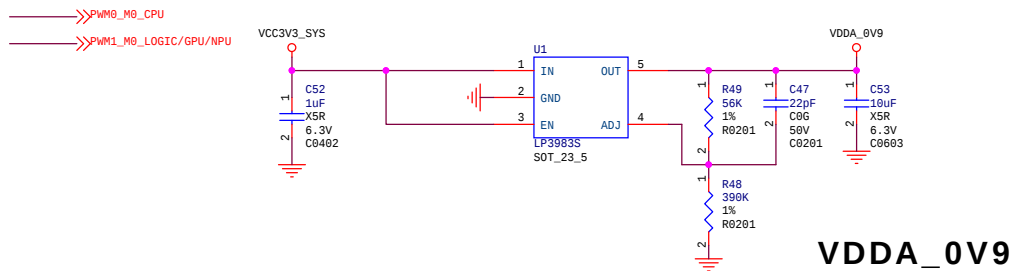
Designed by: <designer> Reviewed by: <Checker> Sheet: 16 of 27

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_V0L_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_V0L_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_V0L_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_V0L_SEL --> Logic=L(Default)

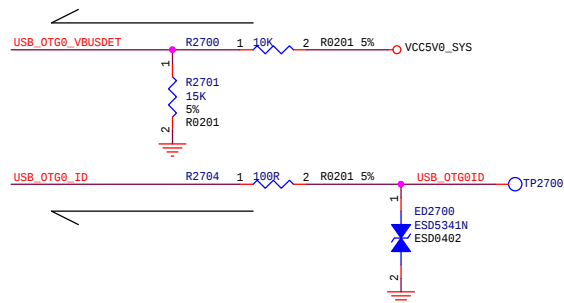


FLASH_V0L_SEL state decided to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

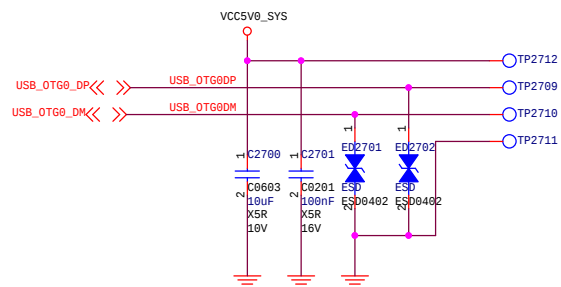


Geniatech Geniatech Electronics Co., Ltd					
Project: RK3566_TABLET_REF					
File: 18.Power_DiscretePower					
Date: Saturday, October 28, 2023	Rev: <Revision>				
Designed by: <designer>	Reviewed by: <Checker>	Sheet: 18 of 27			

USB2.0 OTG



If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability



```

----->>> GMAC1_TXD0
----->>> GMAC1_TXD1
----->>> GMAC1_TXD2
----->>> GMAC1_TXD3
----->>> GMAC1_TXEN
----->>> GMAC1_TXCLK

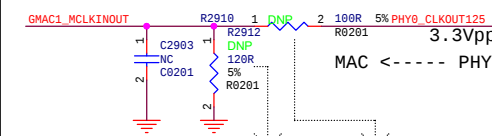
----->>> GMAC1_RXD0
----->>> GMAC1_RXD1
----->>> GMAC1_RXD2
----->>> GMAC1_RXD3
----->>> GMAC1_RXDV_CRS

----->>> GMAC1_RXCLK
----->>> ETH1_REFCLK_0_25M
----->>> GMAC1_MCLKINOUT
-----<<< GMAC1_MDC
-----<<< GMAC1_MDIO

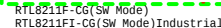
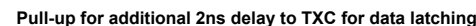
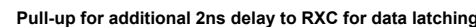
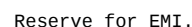
----->>> GMAC1_RSTn

-----<<< GMAC1_INT/PMFR

```

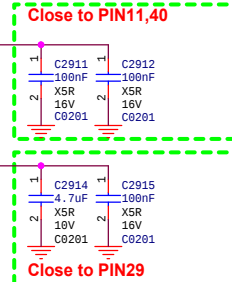
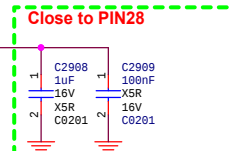


Default	
---------	--



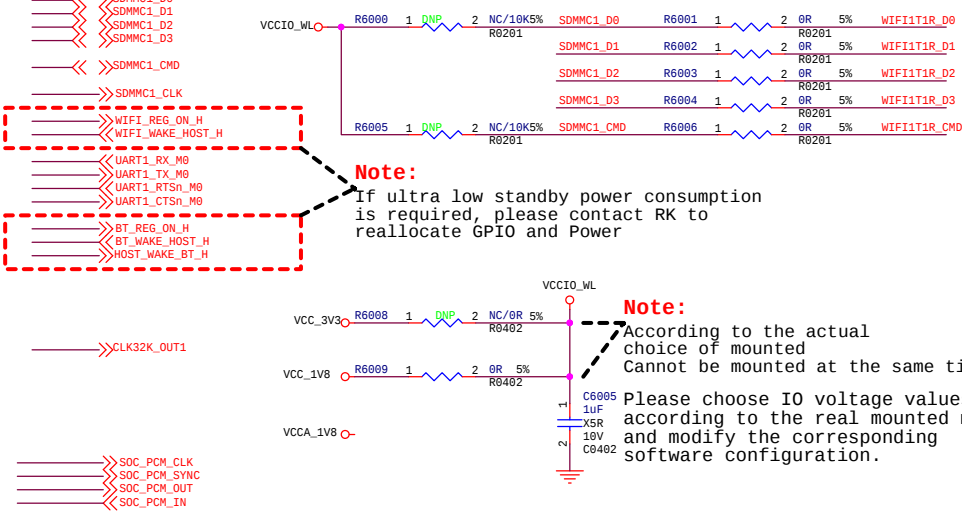
```
CFG_EXT:
1: External Power Source for IO pad
0: Integrated LDO for IO pad

CFG_LD0(1:0)
10: 1.8V
00: 3.3V
```

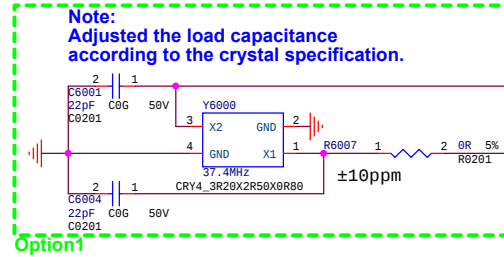
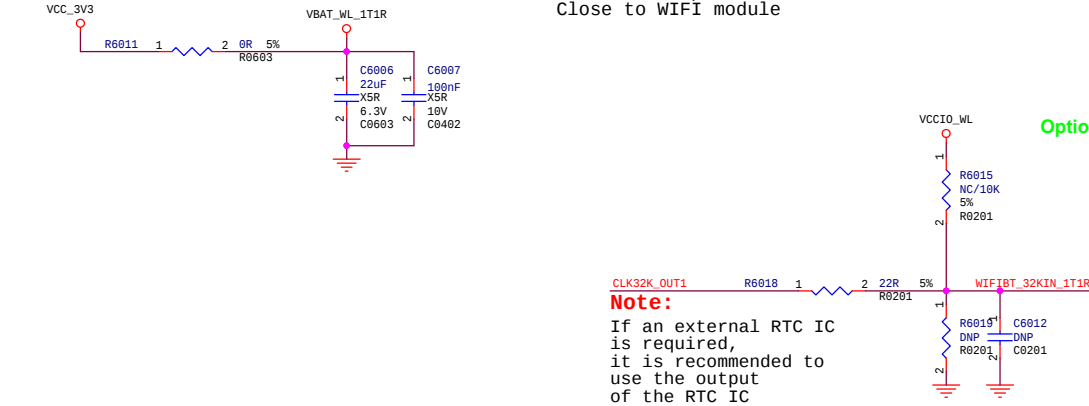


SDIO WIFI/BT MODULE

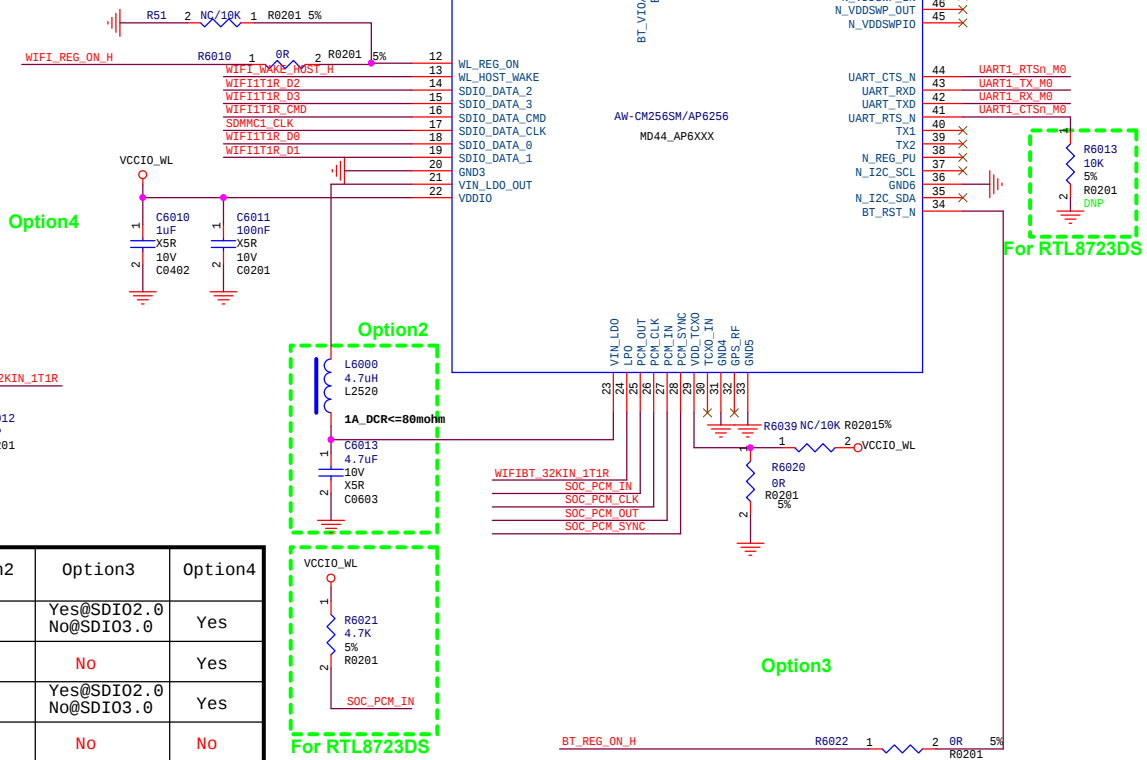
And Giga PHY0 Option



The maximum peak current is 600mA
Close to WIFI module



Using RTL8189ETV/FTV modules, please notice
WIFI REG ON is on pin12 or pin34, choose according to the actual condition.



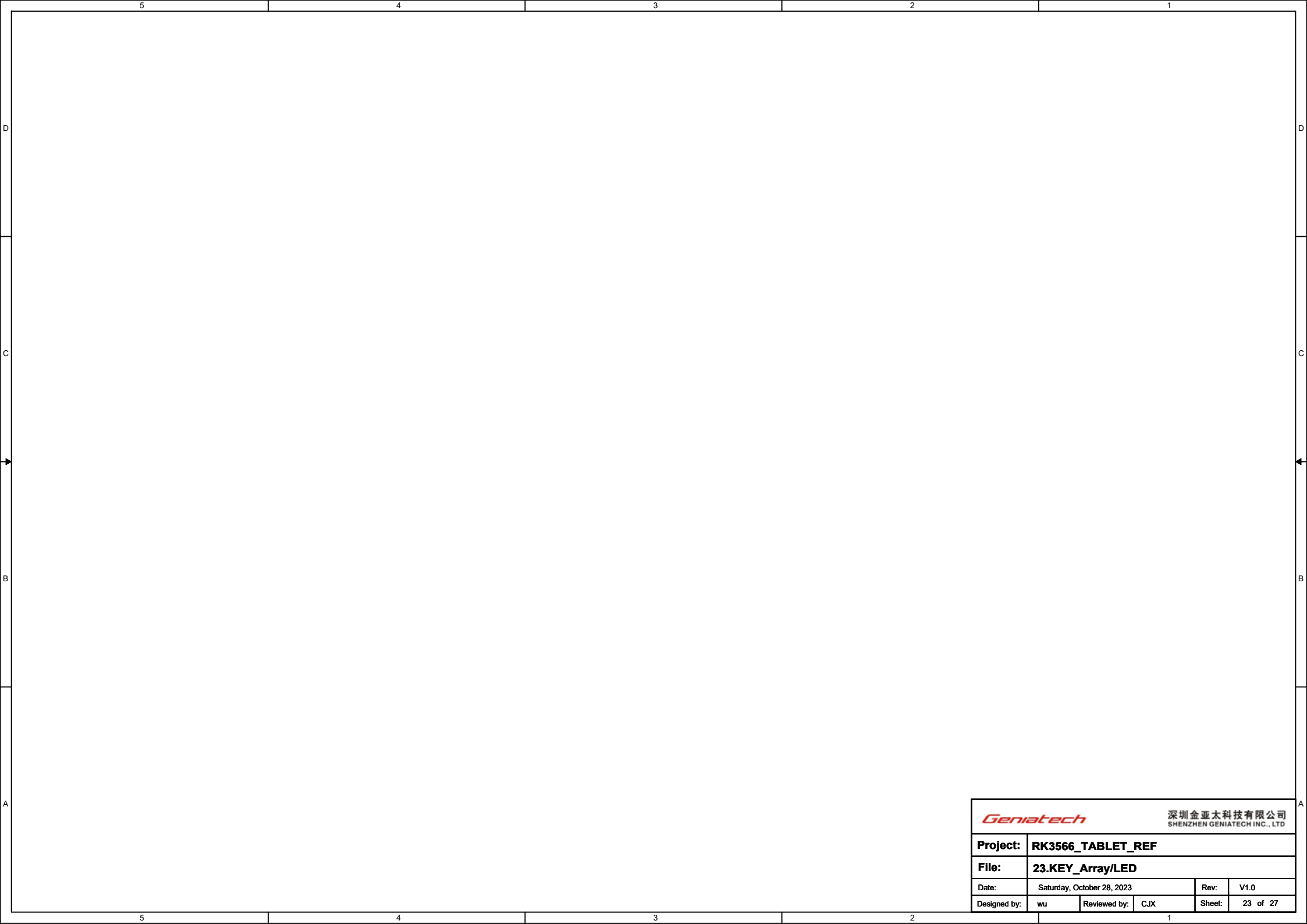
Using RTL8189ETV/FTV modules, please notice
WIFI REG ON is on pin12 or pin34, choose according to the actual condition.

OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHZ							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

			
Project:	RK3566_TABLET_REF		
File:	22.WIFI/BT-SDMMC1_1T1R + UART		
Date:	Saturday, October 28, 2023	Rev:	V1.0
Designed by:	wu	Reviewed by:	cjx
Sheet:	22	of	27

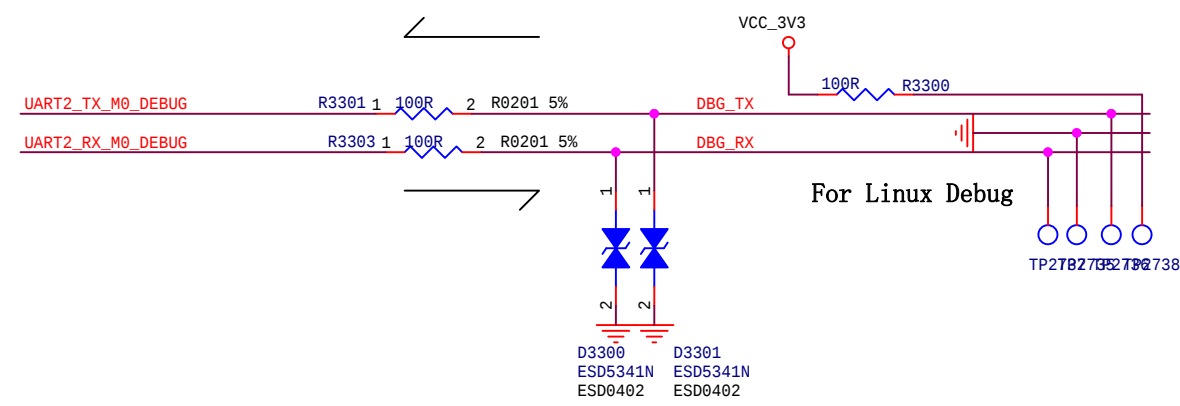
Rockchip Confidential



		深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD			
Project:	RK3566_TABLET_REF				
File:	23.KEY_Array/LED				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	23 of 27

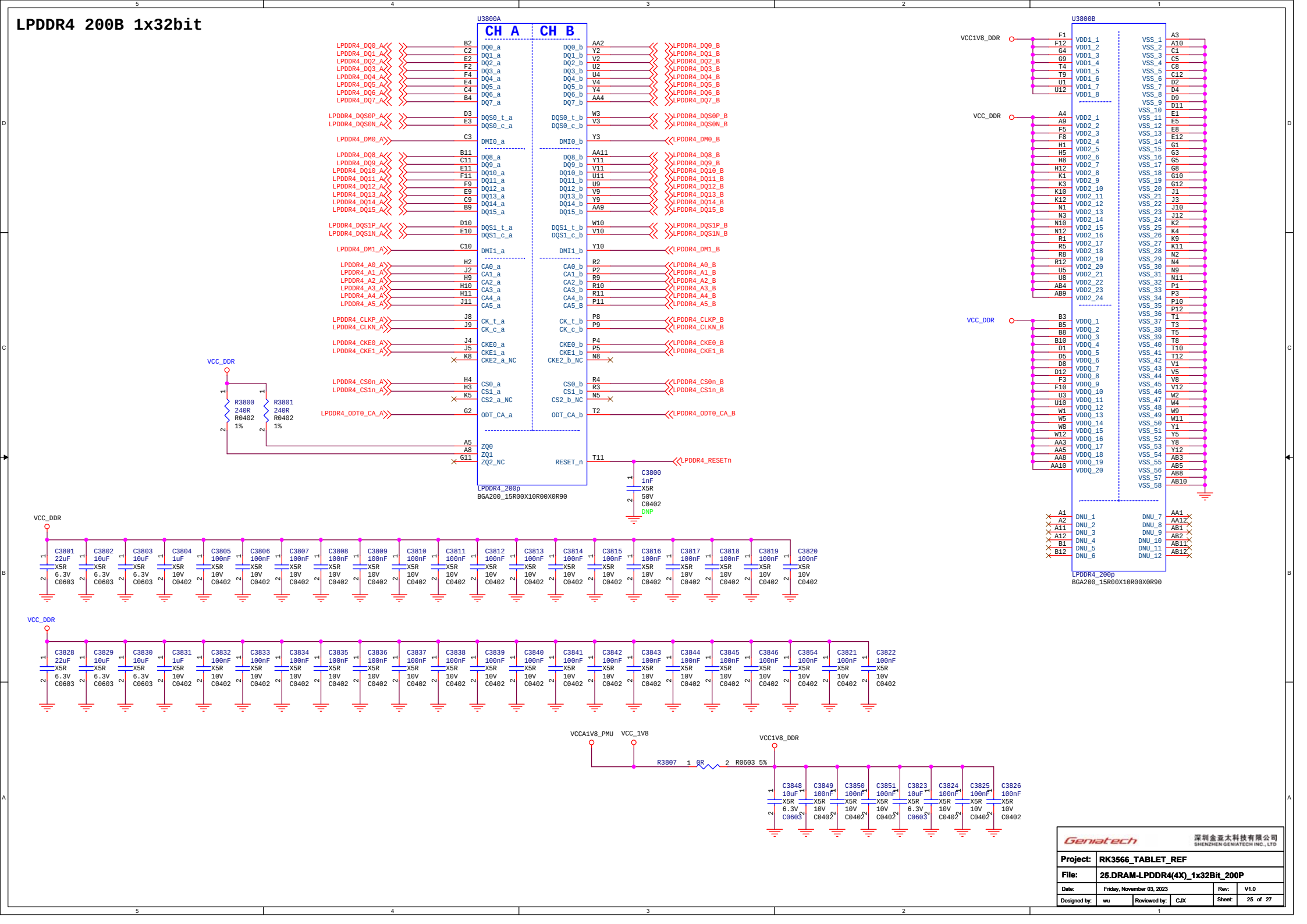
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



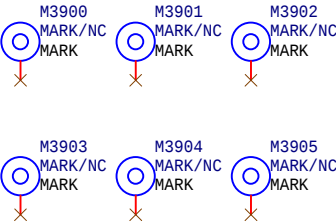
<i>Geniatech</i>		深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD	
Project:	RK3566_TABLET_REF		
File:	24.Debug_UART/IR		
Date:	Saturday, October 28, 2023		Rev: V1.0
Designed by:	wu	Reviewed by: CJX	Sheet: 24 of 27

LPDDR4 200B 1x32bit

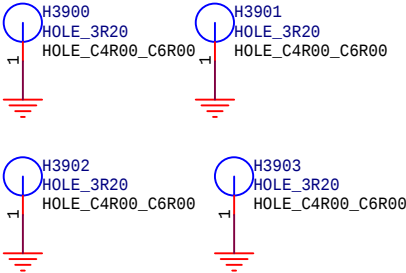


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PCB Mark Point



Mechanical Hole



Heatsink

							
				SHENZHEN GENIATECH INC., LTD			
Project:		RK3566_TABLET_REF					
File:		27.Mark/Hole/Heatsink					
Date:		Saturday, October 28, 2023				Rev:	V1.0
Designed by:		wu	Reviewed by:		CJX	Sheet:	27 of 27