Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2023.08.01	Linta	1: Revision preliminary version;	
V1.1	2023.09.22	Linta	1：修改固定孔大小	

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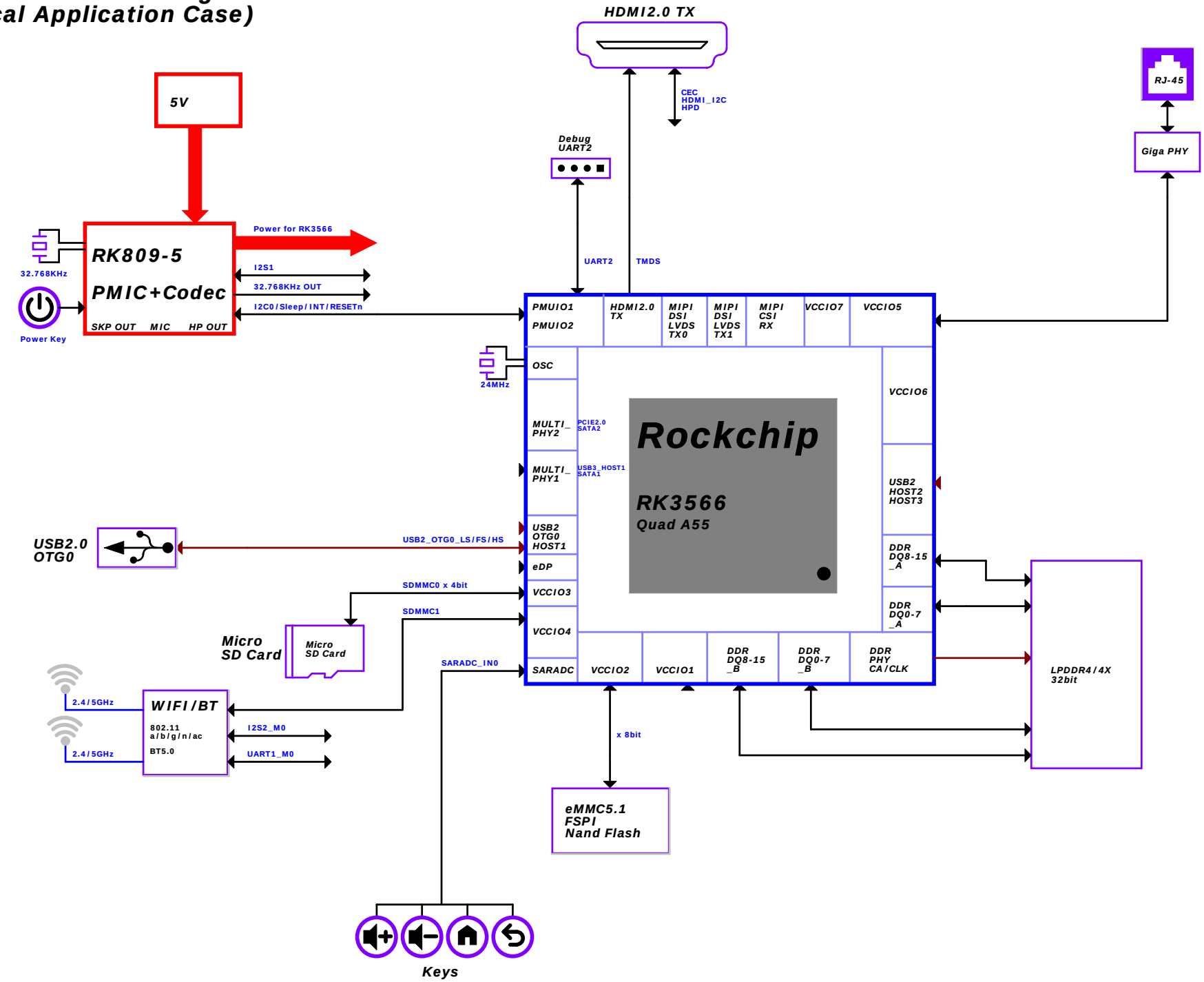
Project:	RK3566_TABLET_REF				
File:	01.Revision_History				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	1 of 27

RK3566 Ref Block Diagram (Typical Application Case)



Project:	RK3566_TABLET_REF
File:	02.Block_Diagram
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Designed by:	au
Reviewed by:	CJK
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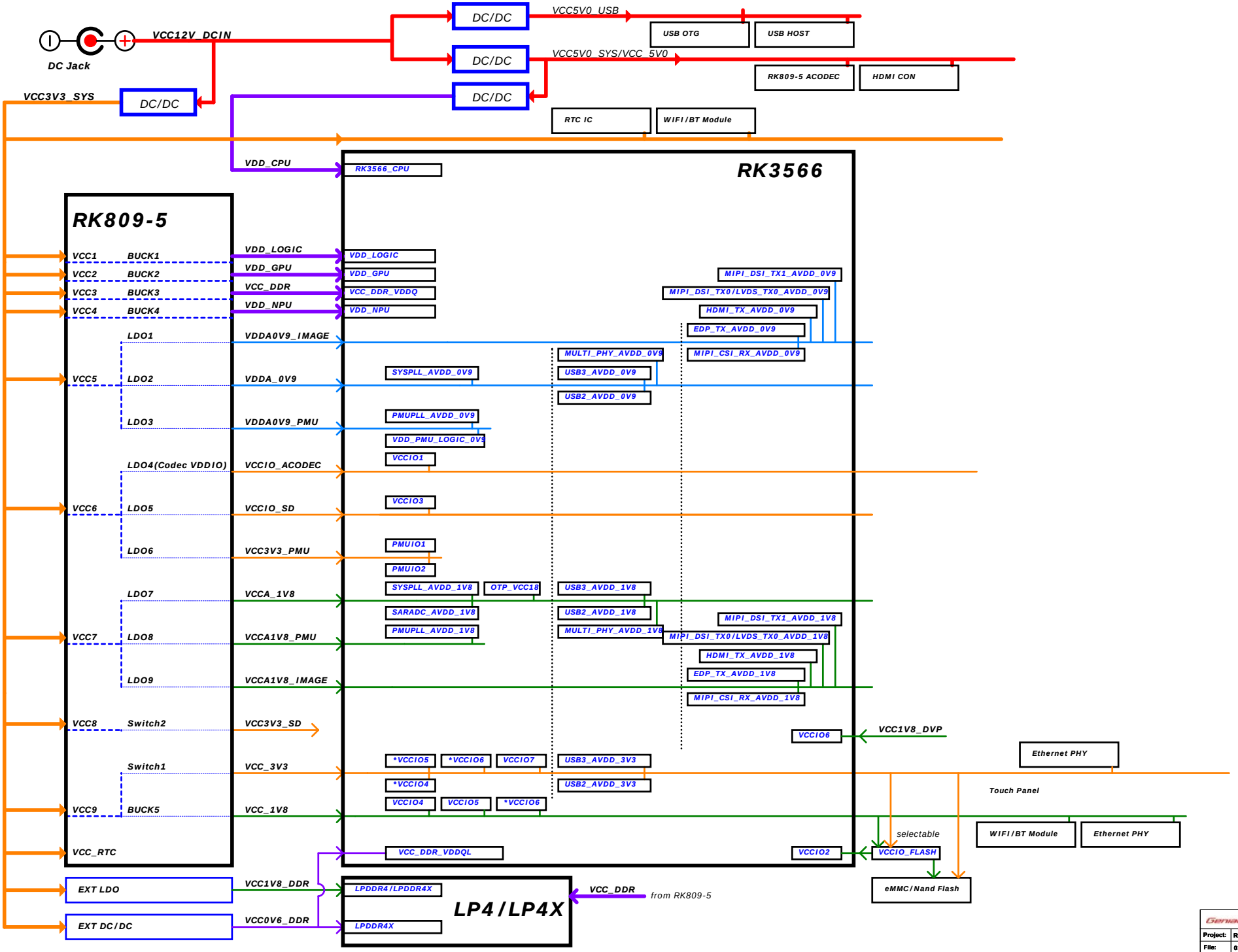
Power Diagram



Project:	RK3566_TABLET_REF
File:	03.Power_Diagram
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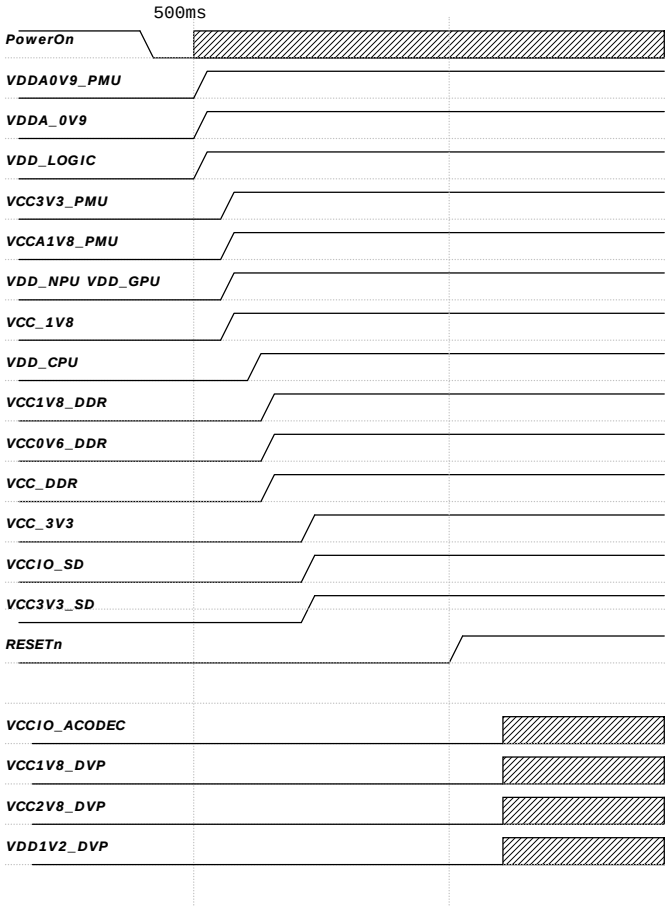
Power Sequence &Power Path assignment



Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETn			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF
VCC_SYS	EXT BUCK	2A	VDD1V2_DVP	N/A	1.2V	ON	OFF

IO Power Domain Map

Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCCA1V8_PMU	VCCA1V8_PMU	1.8V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC_1V8	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

!!! Attention

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Project:	RK3566_TABLET_REF				
File:	04.Power_Sequence/IO_Domain_Map				
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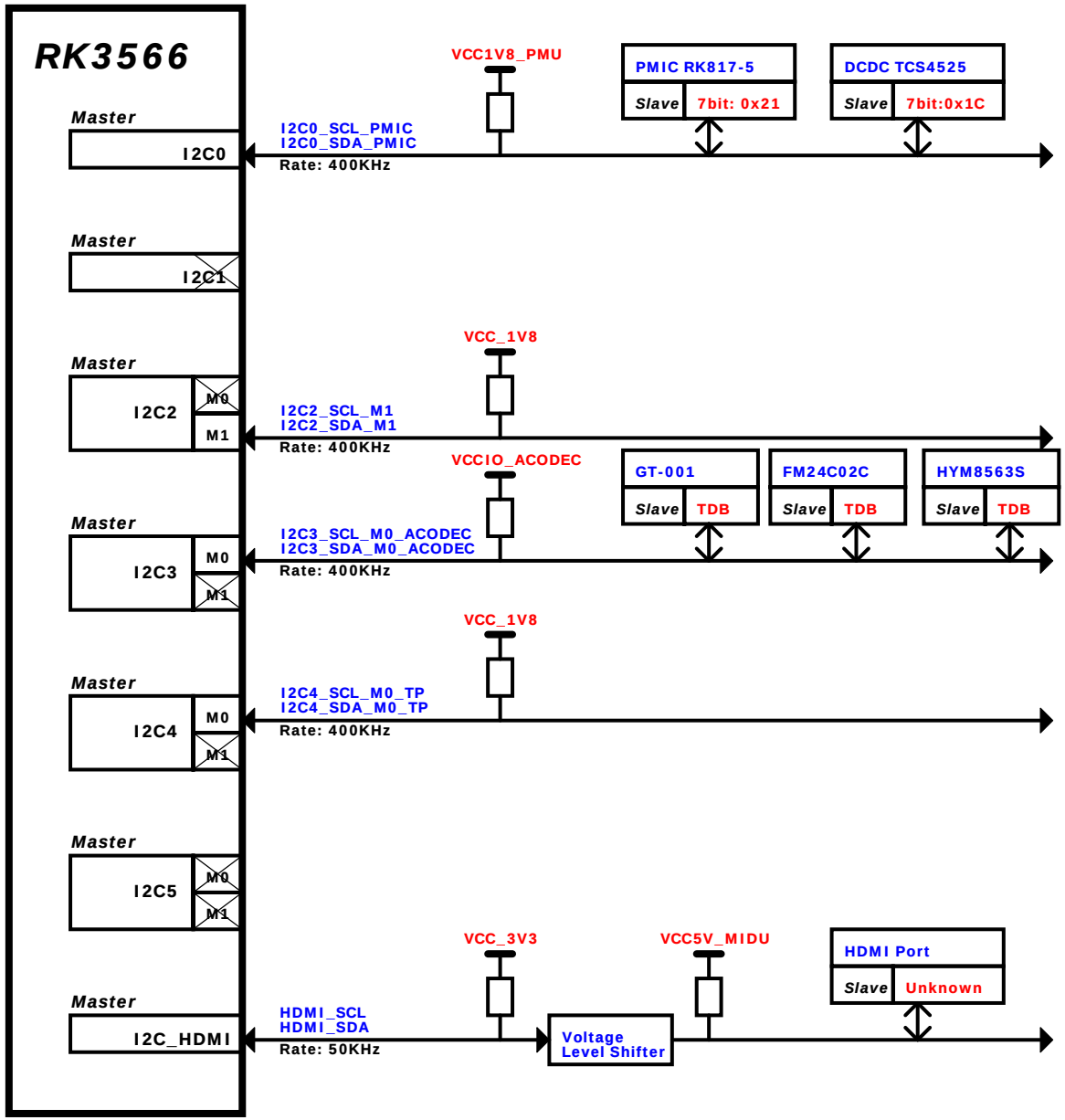
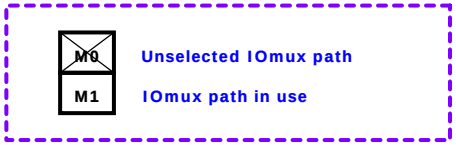
I2C MAP





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Project:	RK3566_TABLET_REF				
File:	05.I2C_Bus_Map				
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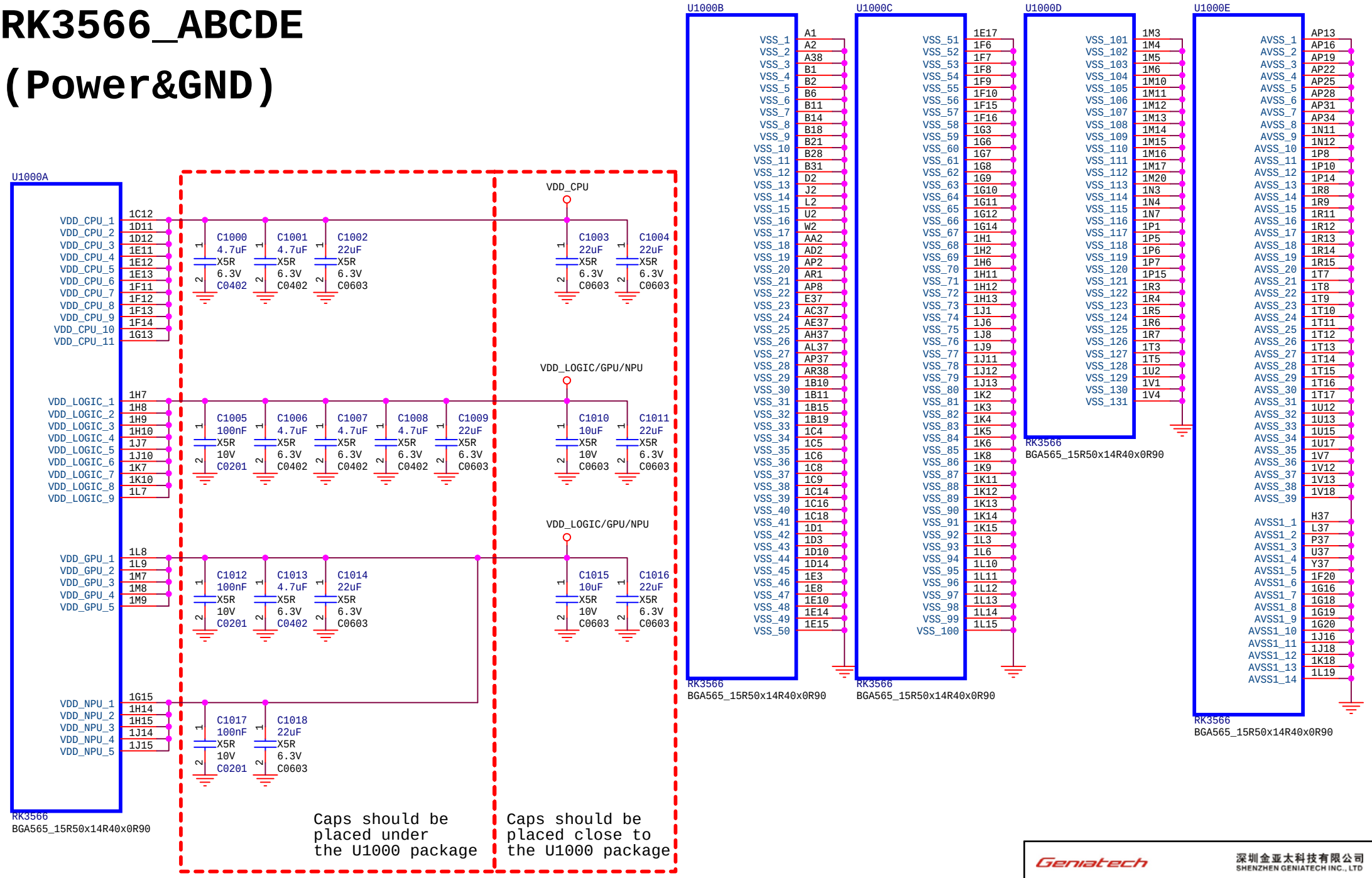
RK3566_ABCDE (Power&GND)



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Project:	RK3566_TABLET_REF				
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RK3566_F(DDR PHY)

U1000F

	DDR4	LPDDR4	DDR3	LPDDR3
G2	DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
F2	DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
F1	DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10
E1	DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9
M2	DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13
K1	DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12
K2	DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8
1E1	DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11
1E2	DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
H2	DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
H1	DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
P2	DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
R1	DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
R2	DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28
T2	DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29
M1	DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26
1F2	DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31
1F1	DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30
1G2	DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27
1G1	DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
N1	DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
N2	DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
B12	DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
B10	DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5
1A8	DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ0
1A7	DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
B13	DDR_DQ4_B	DDR4_DQU8_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2
1A10	DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ7
1B9	DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
1A9	DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ6
1B8	DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0
A13	DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P
A12	DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N
B19	DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
A19	DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
A20	DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22
B20	DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23
A15	DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16
B15	DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17
1C10	DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20
B16	DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21
1A11	DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2
A17	DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P
B17	DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N

Note:
Except DDR3, other DQ sequences can not be swap

	DDR4	LPDDR4	DDR3	LPDDR3
A7 AC8	DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC8
1D2	DDR4_A1	---	DDR3_A2	---	AC1
C1 AC2	DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2
1C3 AC3	DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3
1B6 AC4	DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4
B8 AC5	DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5
B9 AC6	DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6
A10 AC7	DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
E2 AC8	DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8
B7 AC9	DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC9
1A3 AC10	DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
C2 AC11	DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A0	AC11
1B3 AC12	DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
A9 AC13	DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0	AC13
1B1 AC14	DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5	AC14
1C1 AC15	DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---	AC15
1A1 AC16	DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16
1A2 AC17	DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17
1B7 AC18	DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
1A6 AC19	DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4	AC19
1A4	DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20
1C2	DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
B4 AC22	DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE	AC22
A5 AC23	DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP	AC23
B5 AC24	DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN	AC24
B3 AC25	DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25
1A5 AC26	DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1	AC26
1B5 AC27	DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27
AC28	DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28
1C7 AC29	DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29

Note: Sequences can not be swap

DDR_RZQ 1F3 DDR_RZQ

DDR_VREFOUT 1H3 TP1100

	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR3	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	**0.60V**

DDR_VDDQ_1 1D5
DDR_VDDQ_2 1D6
DDR_VDDQ_3 1D7
DDR_VDDQ_4 1D8
DDR_VDDQ_5 1D9
DDR_VDDQ_6 1E4
DDR_VDDQ_7 1F4
DDR_VDDQ_8 1G4

DDR_VDDQL_1 1E6
DDR_VDDQL_2 1E7
DDR_VDDQL_3 1E9
DDR_VDDQL_4 1F5
DDR_VDDQL_5 1G5

DDR_AVSS 1D4

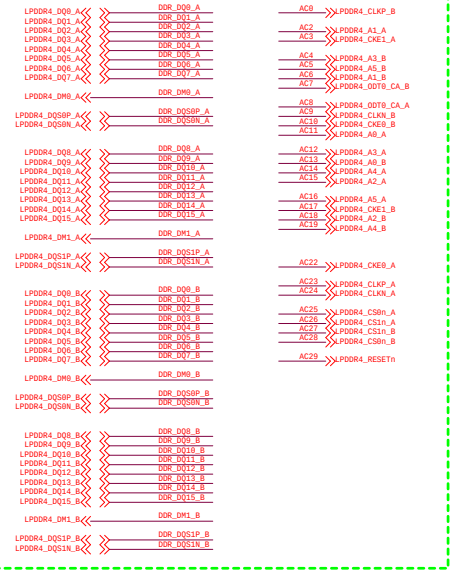
Caps should be placed under the U1000 package

RK3566
BGA565_15R50x14R40x0R90

Note:
Pull up for LPDDR4/LPDDR4X
-->R1100=DNP, R1101=120R;
Pull down for DDR4/DDR3/LPDDR3
-->R1100=120R, R1101=DNP;
The resistor parameter is 120R ±1%.

R1100 120R/1% R0201 1%
R1101 120R/1% R0201 1%
VCC_DDR

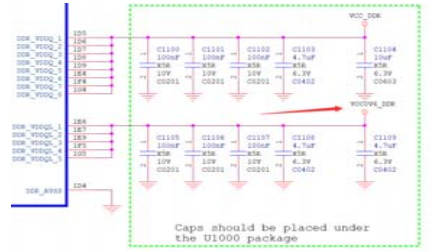
Default: DQ&CA Connection for LPDDR4/LPDDR4X



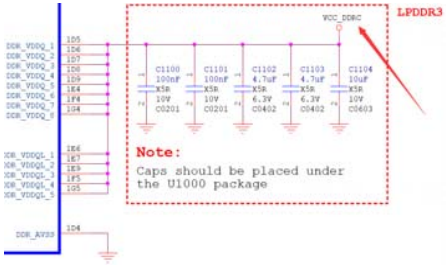
Attention!

For LPDDR4X DDR_VDDQL = 0.6V,
refer to the connection example
For LPDDR3 ultra low power mode,
DDR_VDDQ&DDR_VDDQL connect to VCC_DDRC

Note:
LPDDR4x mode:
Pin 1E6,1E7,1E9,1F5,1G5 connected to VCC0V6_DDR power supply
For example



Note:
LPDDR3 ultra low power mode:



Project:	RK3566_TABLET_REF		
File:	07.RK3566_DDR_PHY		
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Designed by:	wu	Reviewed by:	CJX
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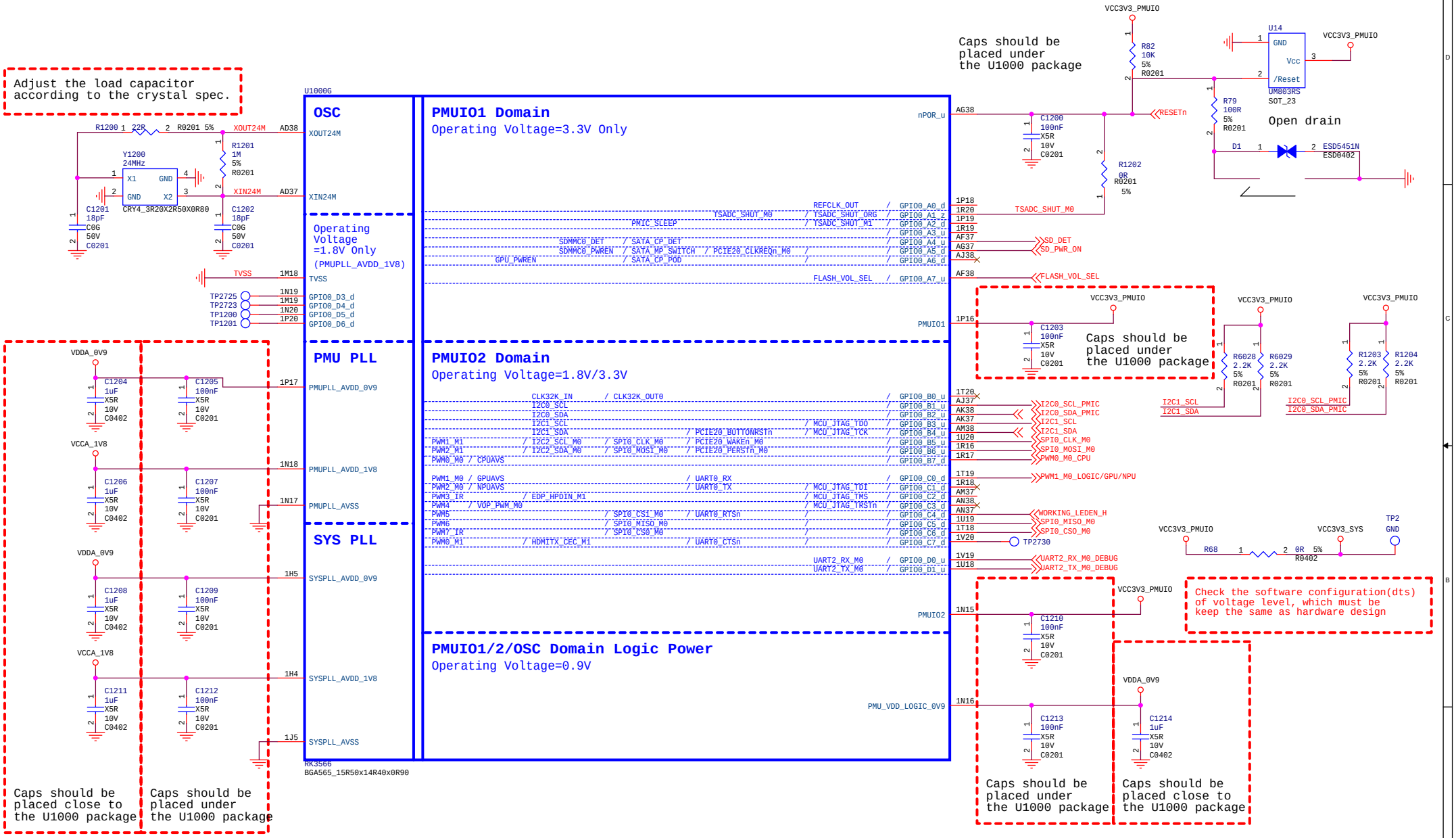
RK3566_G(OSC/PLL/PMUIO1/2)



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Project:	RK3566_TABLET_REF				
File:	08.RK3566_OSC/PLL/PMUIO				
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RK3566_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/	GPIO1_B4_u	A32
EMMC_D1	/ FLASH_D1	/	GPIO1_B5_u	B27
EMMC_D2	/ FLASH_D2	/	GPIO1_B6_u	B32
EMMC_D3	/ FLASH_D3	/	GPIO1_B7_u	B29
EMMC_D4	/ FLASH_D4	/	GPIO1_C0_u	B33
EMMC_D5	/ FLASH_D5	/	GPIO1_C1_u	A30
EMMC_D6	/ FLASH_D6	/	GPIO1_C2_u	B30
EMMC_D7	/ FLASH_D7	/	GPIO1_C3_u	A33
EMMC_CMD	/ FLASH_WRn	/	GPIO1_C4_u	A27
EMMC_CLKOUT	/ FLASH_DQS	/	GPIO1_C5_d	A29
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/	GPIO1_C6_d	1A16
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/	GPIO1_C7_d	1B16
	FSPI_CLK / FLASH_ALE	/	GPIO1_D0_d	1A15
	FSPI_D0 / FLASH_RDY	/	GPIO1_D1_u	1A17
	FSPI_D1 / FLASH_RDn	/	GPIO1_D2_u	1A18
	FSPI_CS0n / FLASH_CS0n	/	GPIO1_D3_u	1B17
	FSPI_D3 / FLASH_CS1n	/	GPIO1_D4_u	1C15
				1C13

Default is determined by Pin FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2

RK3566
BGA565_15R50x14R40x0R90

A32 eMMC_D0/FLASH_D0
B27 eMMC_D1/FLASH_D1
B32 eMMC_D2/FLASH_D2
B29 eMMC_D3/FLASH_D3
B33 eMMC_D4/FLASH_D4
A30 eMMC_D5/FLASH_D5
B30 eMMC_D6/FLASH_D6
A33 eMMC_D7/FLASH_D7
A27 eMMC_CMD/FLASH_WRn
A29 R1300 1 22R 2 R0201 5% eMMC_CLKOUT/FLASH_DQS
1A16 eMMC_DATA_STROBE/FLASH_CLE
1B16 eMMC_RSTn/FSPI_D2/FLASH_WPn
1A15 TP1302
1A17 TP1303
1A18 TP1304
1B17 TP1305
1C15 TP1306

VCCIO_FLASH
1C13 C1300 100nF X5R 10V C0201

Caps should be placed under the U1000 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

eMMC_D0/FLASH_D0 TP1300 eMMC_D0/FLASH_D0
TP1301 GND

1. eMMC or Nand Flash:
   Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.

2. SPI Flash:
   Short 'FSPI_CLK/FLASH_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

RK3566_J(VCCIO3 Domain)

U1000J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1 / SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/	GPIO1_D5_u	1E20
PWM9_M1 / SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/	GPIO1_D6_u	1F19
SDMMC0_D2	/ ARM_JTAG_TCK/ UART5_CTSn_M0	/	GPIO1_D7_u	1D20
SDMMC0_D3	/ ARM_JTAG_TMS/ UART5_RTSn_M0	/	GPIO2_A0_u	1F18
PWM10_M1 / SDMMC0_CMD	/ UART5_RX_M0	/	GPIO2_A1_u	1E19
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/	GPIO2_A2_d	G38
				1F17

VCCIO3

RK3566
BGA565_15R50x14R40x0R90

1E20 SDMMC0_D0
1F19 SDMMC0_D1
1D20 SDMMC0_D2
1F18 SDMMC0_D3
1E19 SDMMC0_CMD
G38 R1301 1 22R 2 R0201 5% SDMMC0_CLK

VCCIO_SD
1F17 C1301 100nF X5R 10V C0201

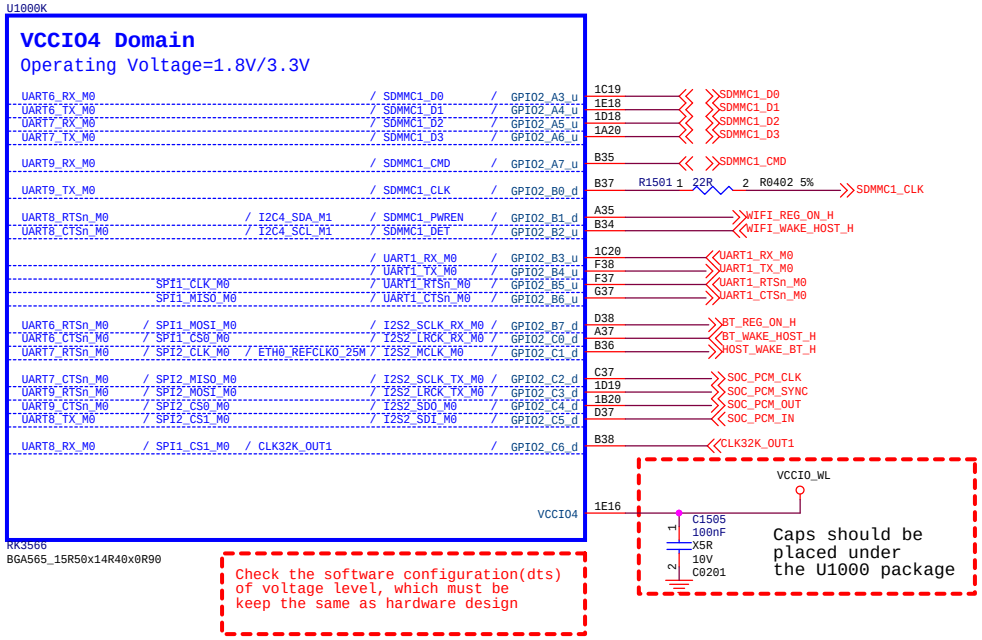
Caps should be placed under the U1000 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

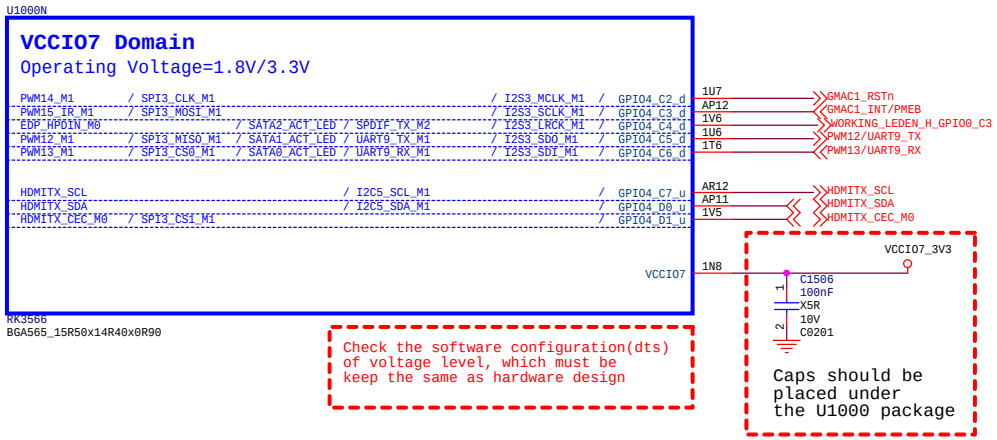
VCC_1V8 R6034 2 NC/0R 1 R0402 5% VCCIO_SD
VCC_3V3 R6035 2 0R DNP 1 R0402 5%
C6014 1uF X5R 10V C0402

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	09.RK3566_FlashSDController				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	9 of 27

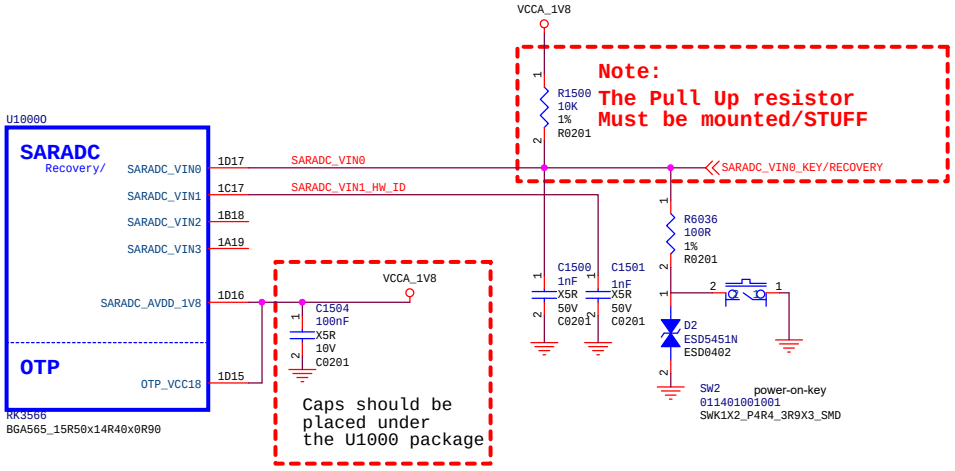
RK3566_K(VCCIO4 Domain)



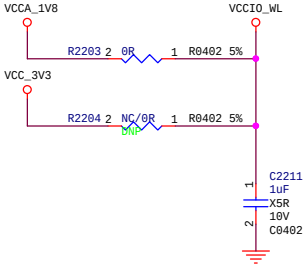
RK3566_N(VCCIO7 Domain)



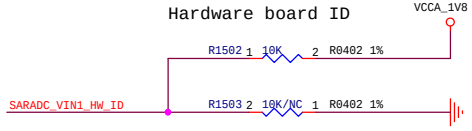
RK3566_O(SARADC/OTP)

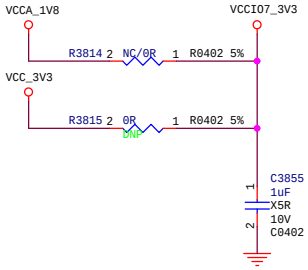


VCCIO_WL



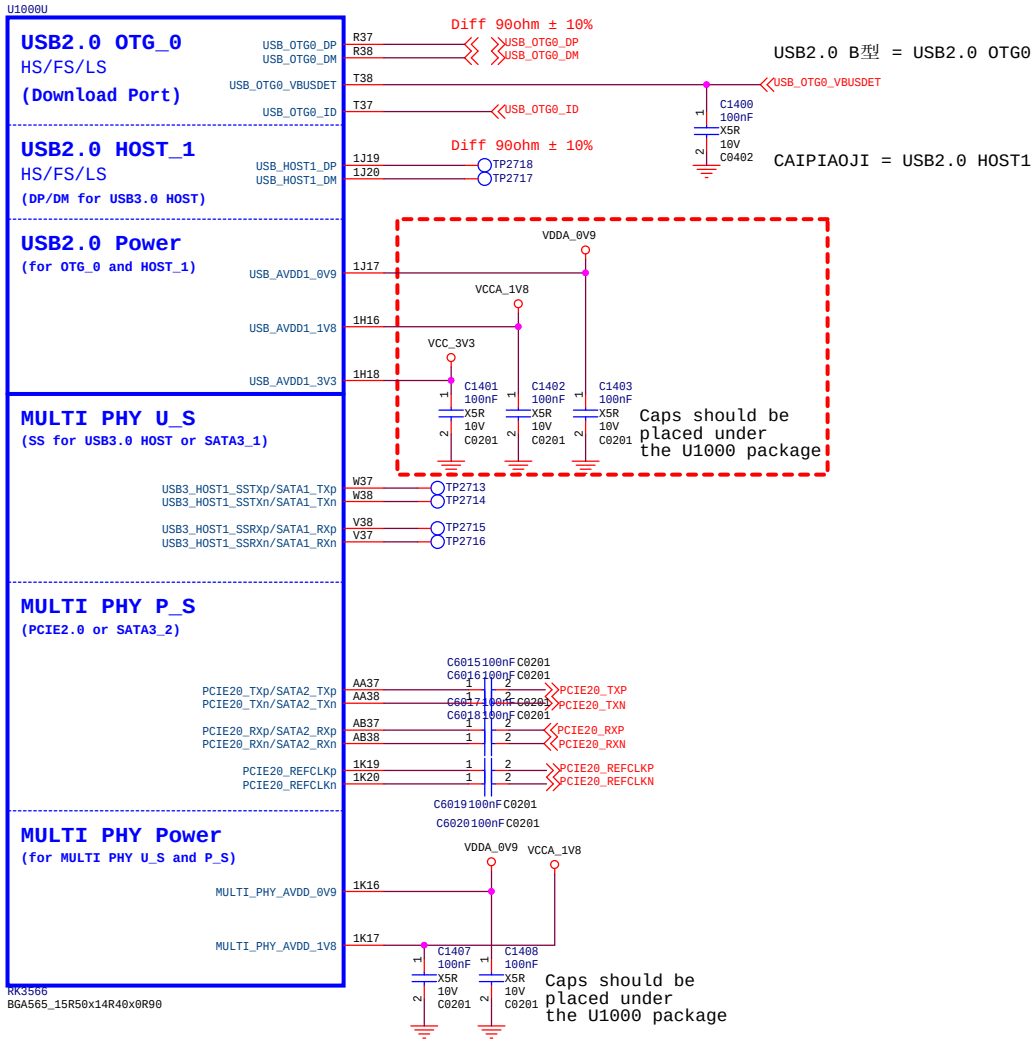
SARADC_VIN1_HW_ID	Rup	Rdown	ADC	
Version_1	10K	DNP	1023	1.8V
Version_2	20K	100K	852	1.5V
Version_3	18K	36K	681	1.2V
Version_4	51K	51K	512	0.9V
Version_5	36K	18K	340	0.6V
Version_6	100K	20K	170	0.3V
Version_7	DNP	10K	0	0V



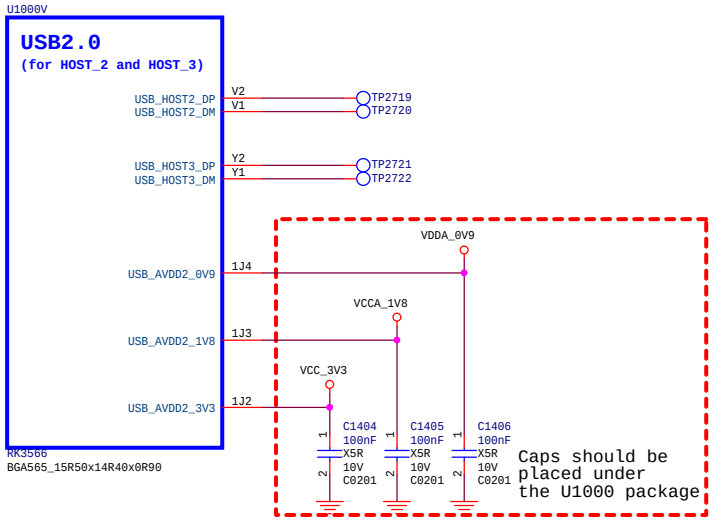


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	10.RK3566_SARADC/GPIO				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	10 of 27

RK3566_U(USB3.0/PCIe2.0x1/SATA)

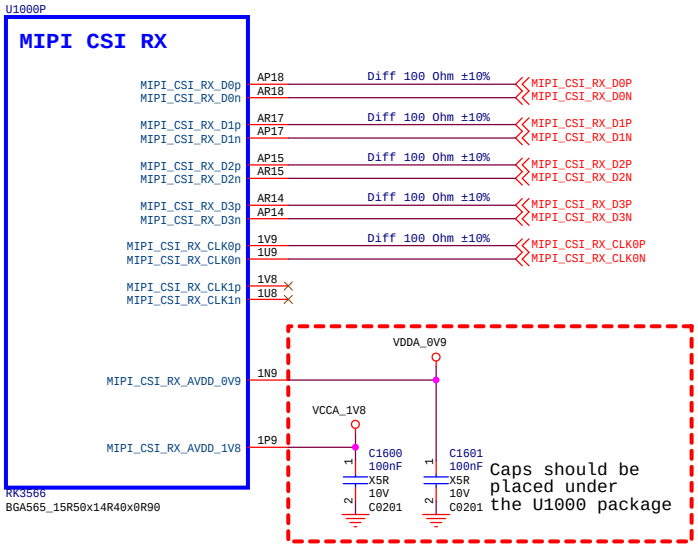


RK3566_V(USB2.0 HOST)



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	11.RK3566_USB/PCIe/SATA_PHY				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	11 of 27

RK3566_P(MIPI_CSI_RX)



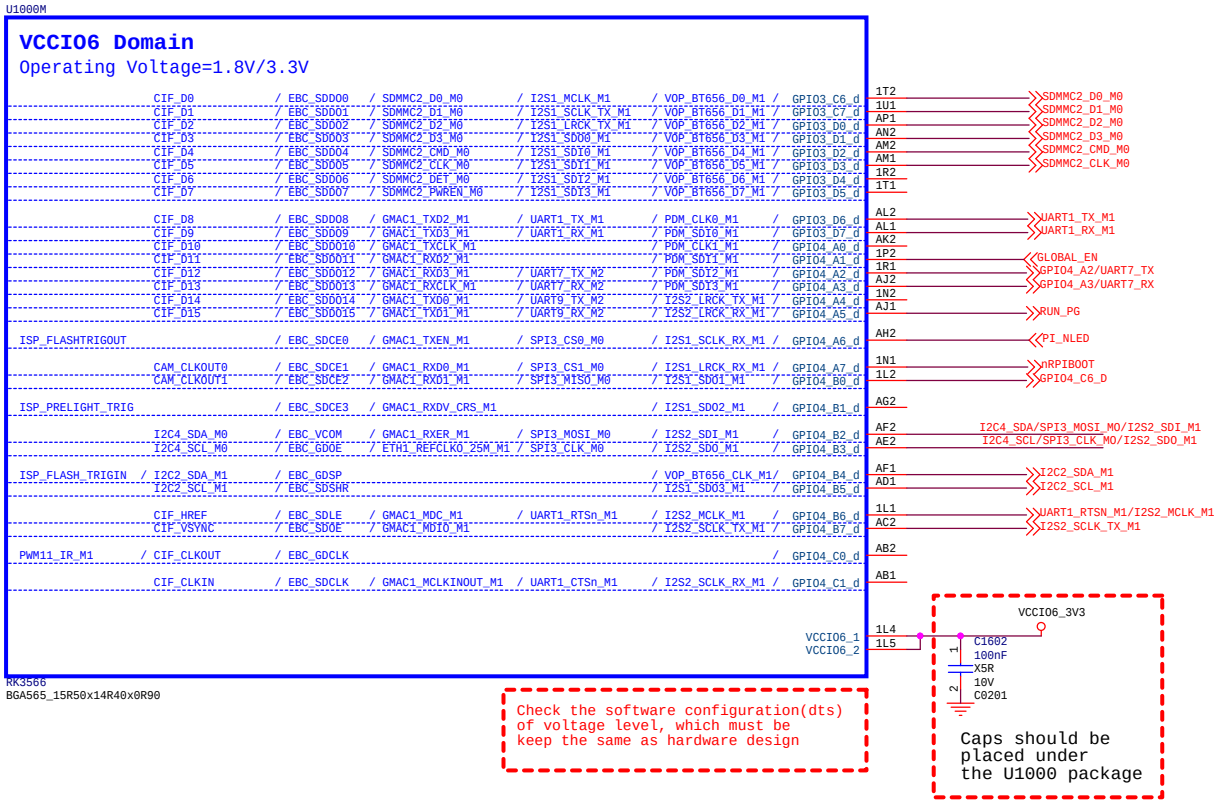
Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Usage of CIF Interface				
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

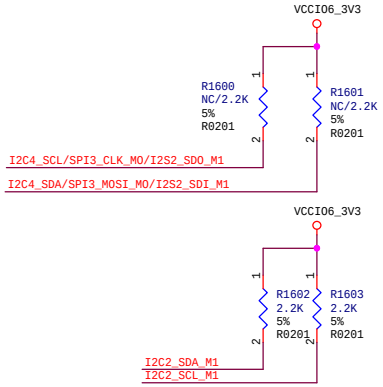
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

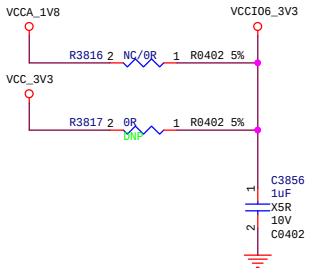
BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

RK3566_M(VCCIO6 Domain)



Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

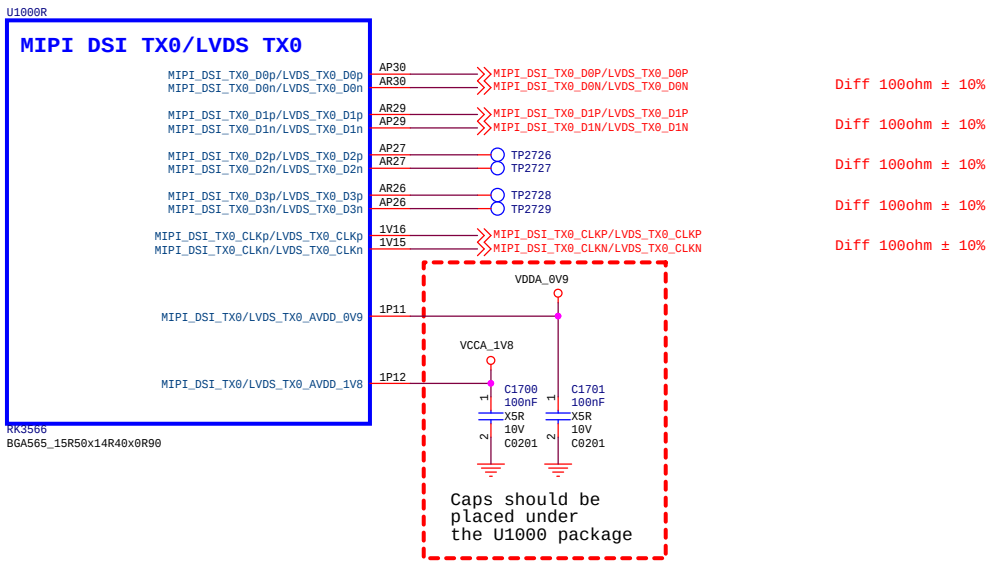




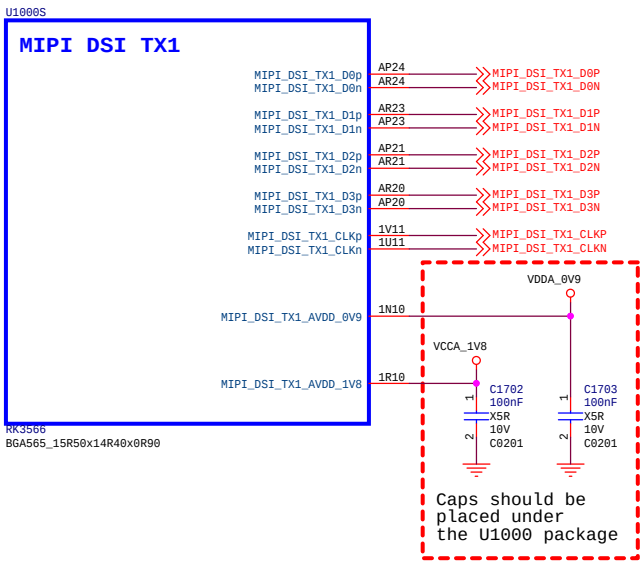
Note:
default VCCIO of Camera is 1.8V

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	12.RK3566_VI_Interface				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	12 of 27

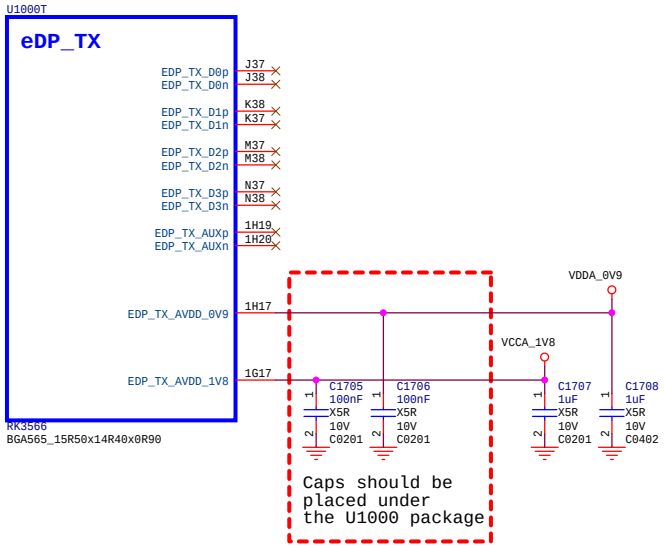
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



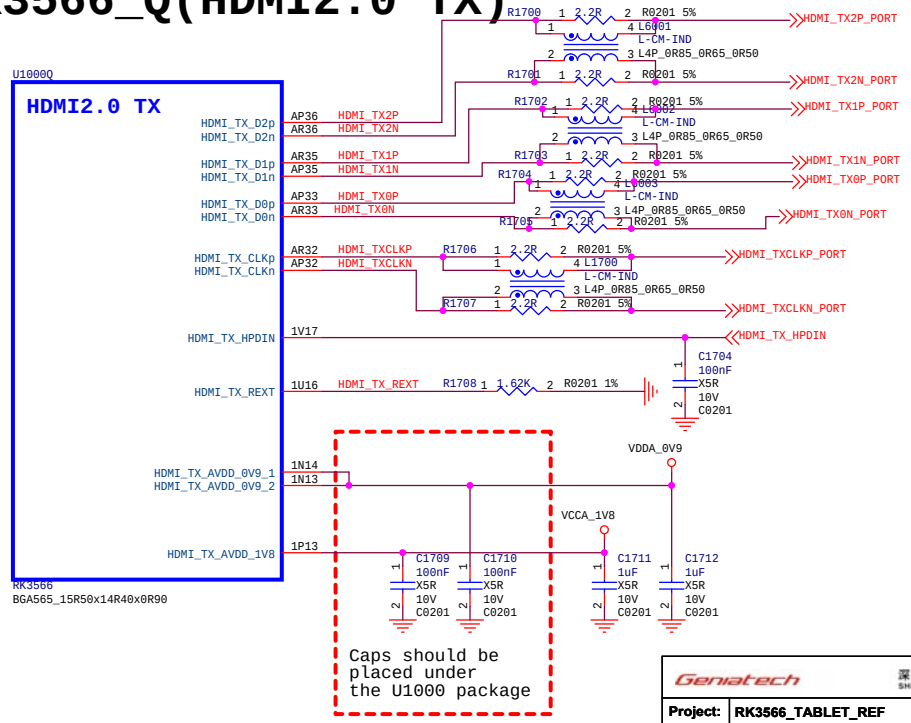
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	13.RK3566_VO_Interface_1				
Date:	Monday, October 30, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	13 of 27

RK3566_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0 / SPI1_CS0_M1			SDMMC2_D0_M1	GPIO3_A1_d
	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
PWM8_M0	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1		GPIO3_B1_d
PWM9_M0	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1		GPIO3_B2_d
	VOP_BT1120_D9 / I2C5_SCL_M0	GMAC1_RXDV_CRS_M0		PDM_SDI0_M2	GPIO3_B3_d
	VOP_BT1120_D10 / I2C5_SDA_M0	GMAC1_RXER_M0		PDM_SDI1_M2	GPIO3_B4_d
PWM10_M0	VOP_BT1120_D11 / I2C3_SCL_M1	GMAC1_TXD0_M0			GPIO3_B5_d
PWM11_IR_M0	VOP_BT1120_D12 / I2C3_SDA_M1	GMAC1_TXD1_M0			GPIO3_B6_d
PWM12_M0		GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
PWM13_M0		GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
	VOP_BT1120_D13 / SPI1_MOSI_M1		PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
	VOP_BT1120_D14 / SPI1_MISO_M1		UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
	VOP_BT1120_D15 / SPI1_CLK_M1		UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3566
BGA565_15R50x14R40x0R90

1U5
AR10 — R1800 1 22R 2 R0402 5% — GMAC1_TXD2
AP10 — R1801 1 22R 2 R0402 5% — GMAC1_TXD3
AR9 — GMAC1_RXD2
AP9 — GMAC1_RXD3
1U4 — R1802 1 22R 2 R0402 5% — GMAC1_TXCLK
1V3 — GMAC1_RXCLK

AR7 — R1803 1 NC/22R 2 R0402 5% — ETH1_REFCLKO_25M
AP7 — GMAC1_RXD0
AR6 — GMAC1_RXD1
AP6 — GMAC1_RXDV_CRS
1U3
1T4 — R1804 1 22R 2 R0402 5% — GMAC1_TXD0
1V2 — R1805 1 22R 2 R0402 5% — GMAC1_TXD1
AP5 — R1806 1 22R 2 R0402 5% — GMAC1_TXEN

AR4 — GMAC1_MCLKINOUT
AP4
AP3
AR2

1P3 — GMAC1_MDC
1P4 — GMAC1_MDIO

VCCA_1V8
1N5
1N6
C1800 100nF X5R 10V C0201

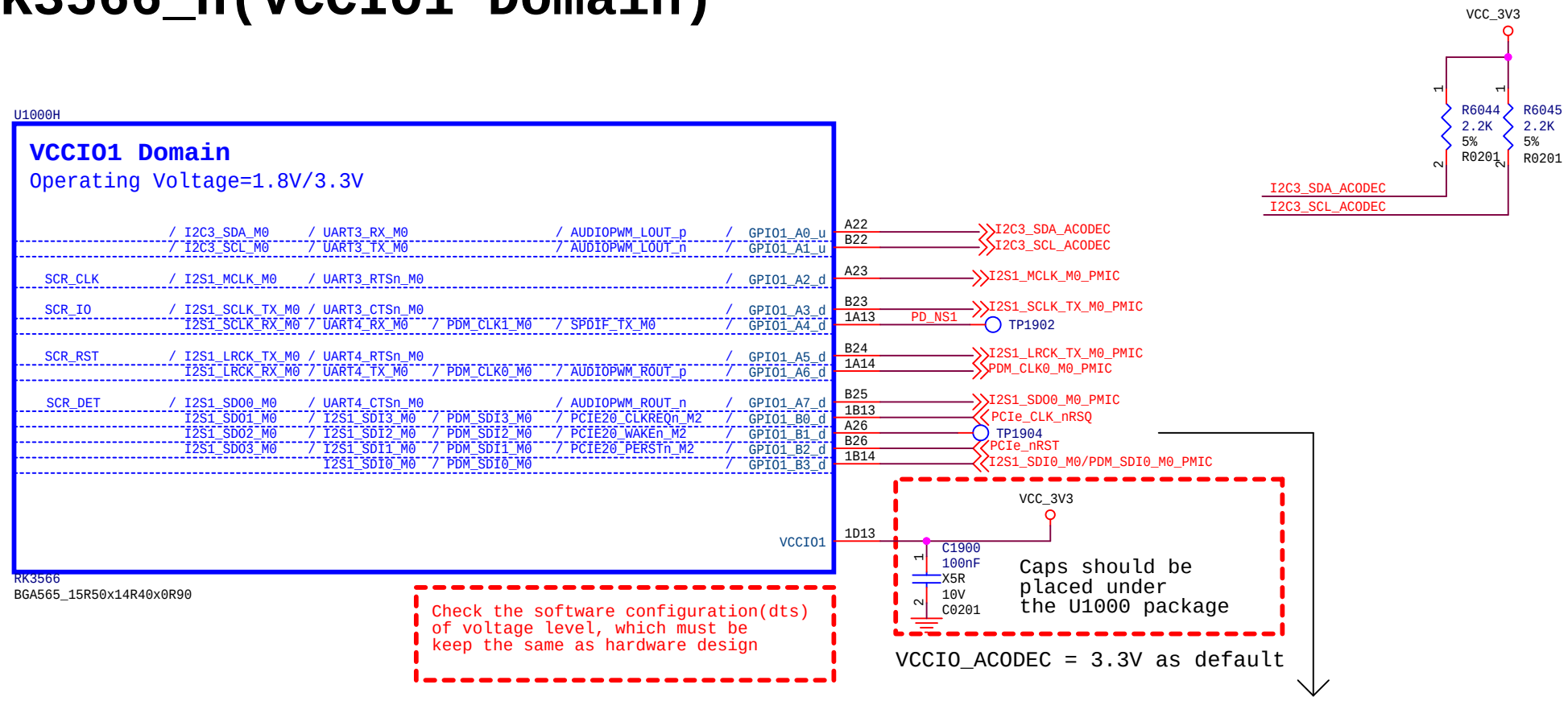
Caps should be placed under the U1000 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Project:	RK3566_TABLET_REF				
File:	14.RK3566_VO_Interface_2				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	14 of 27

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD

RK3566_H(VCCIO1 Domain)



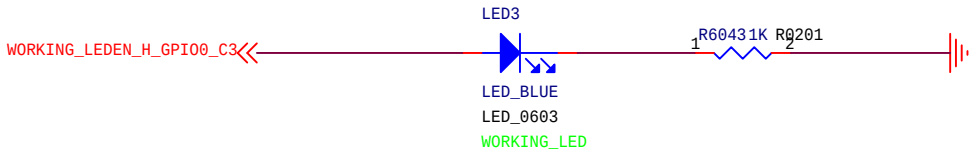
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

VCCIO_ACODEC = 3.3V as default

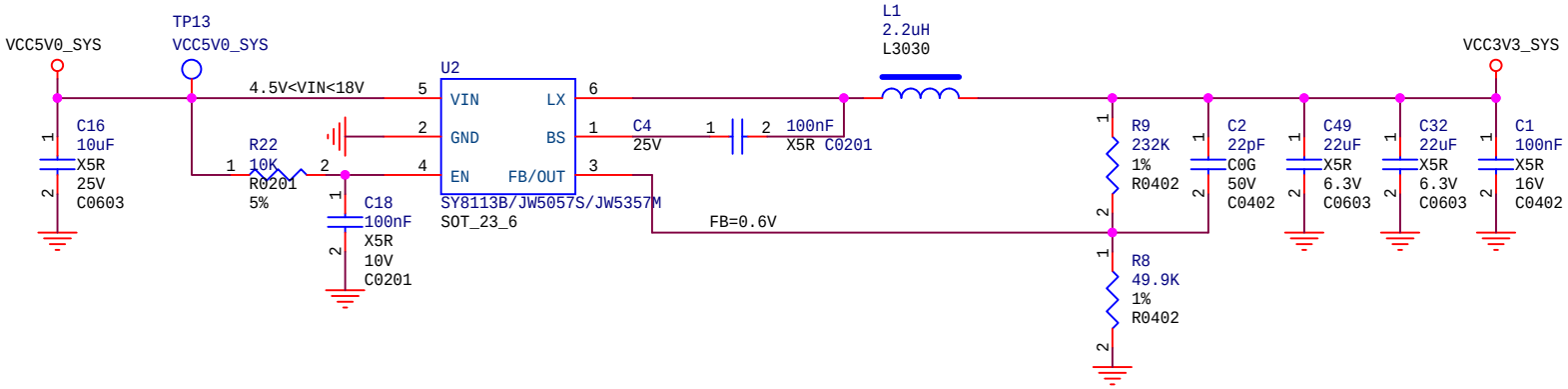
Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	15.RK3566_Audio_Interface				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	15 of 27

12V/3A DCIN

VCC5V0_SYS



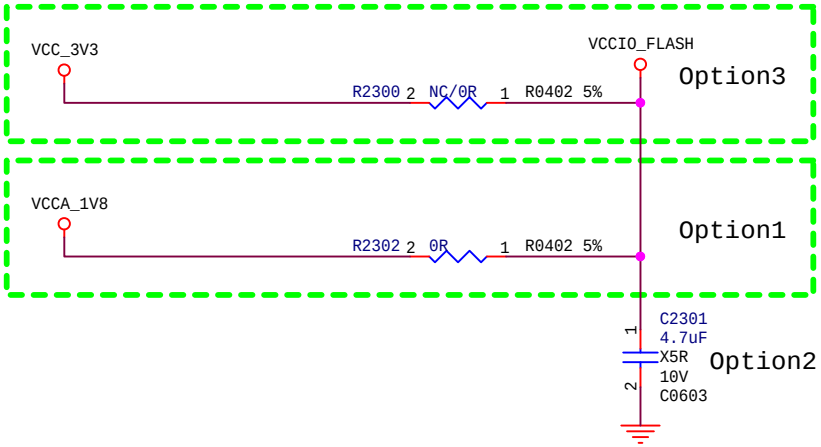
VCC3V3_SYS

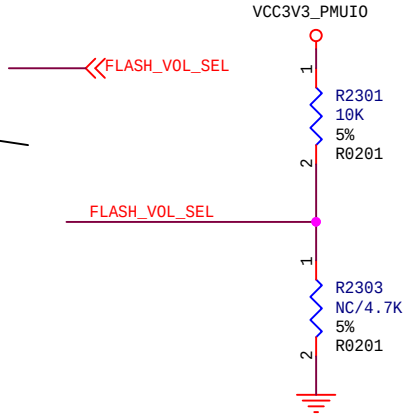


Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_TABLET_REF				
File:	16.Power_DC IN 5V				
Date:	Saturday, October 28, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	16 of 27

Flash Power Manage

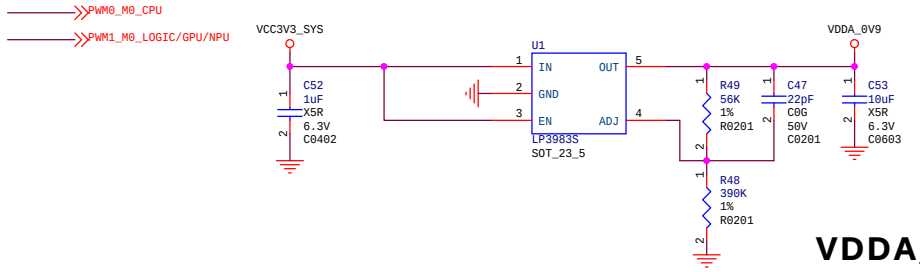
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



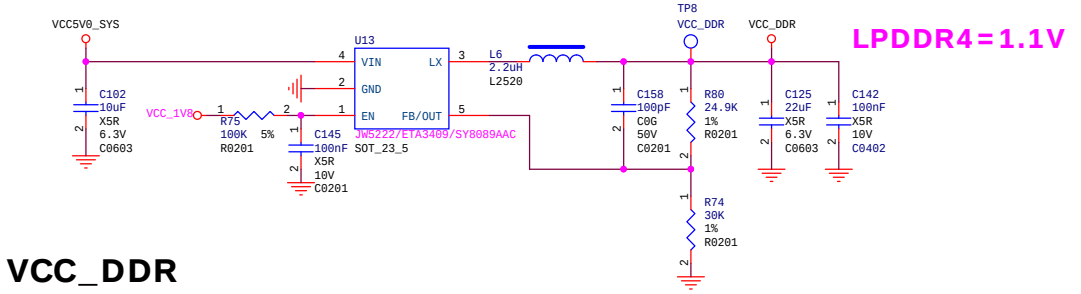


FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	17.Power_Flash_Power_Manage				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	17 of 27

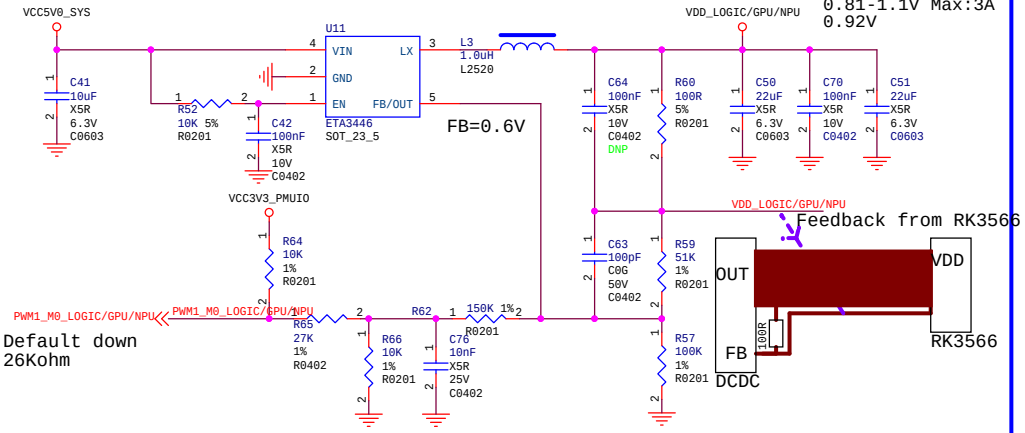


VDDA_0V9

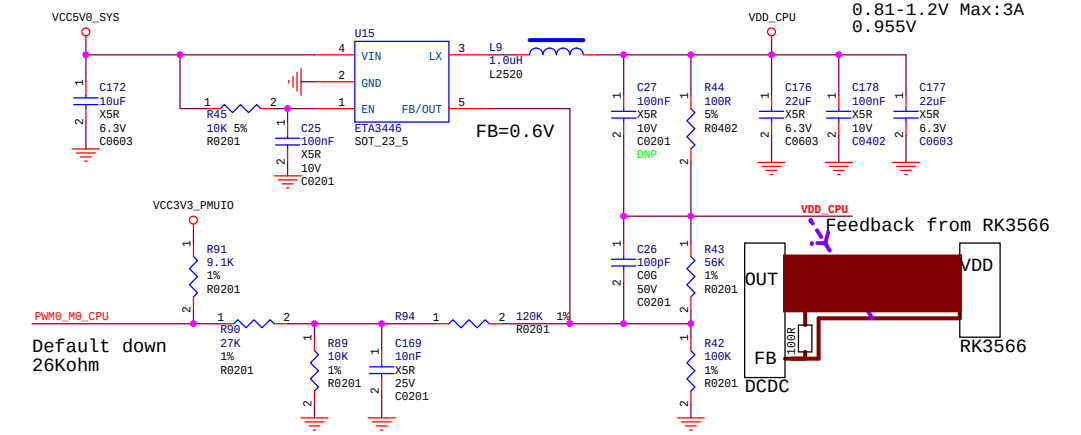


VCC_DDR

VDD_LOGIC/GPU/NPU

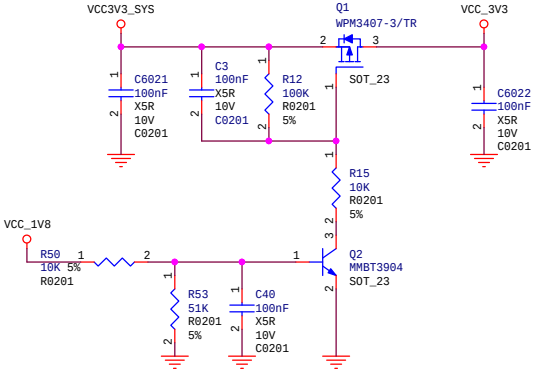


VDD_CPU

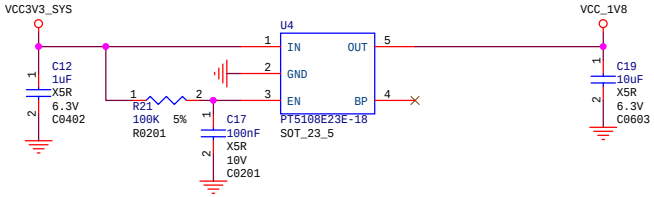


VCC_3V3

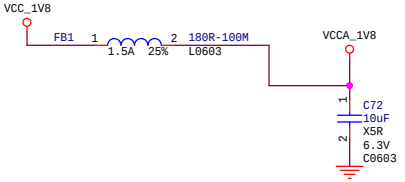
VCC_3V3 power supply has power on timing requirements, can not be deleted!



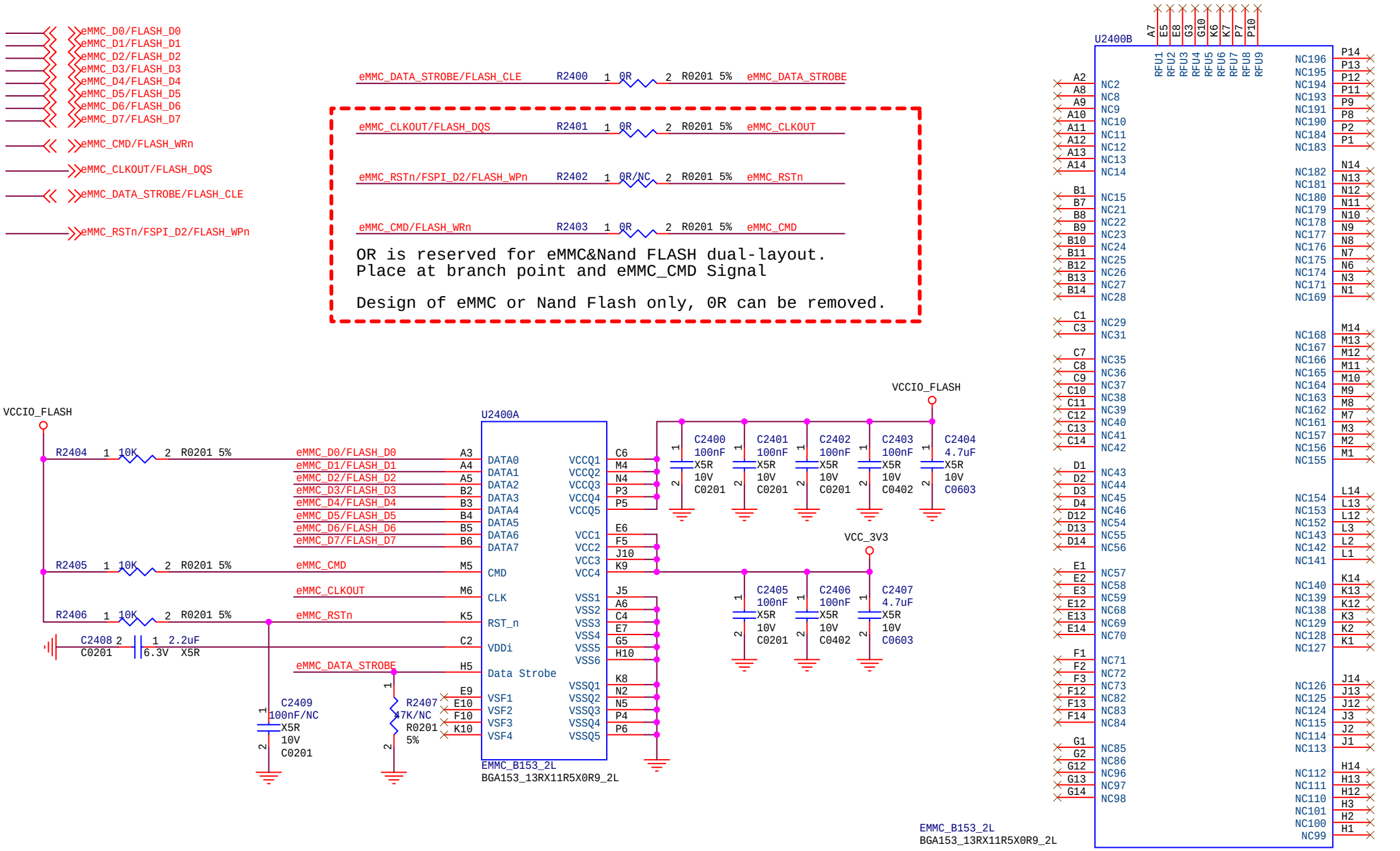
VCC_1V8



VCCA_1V8

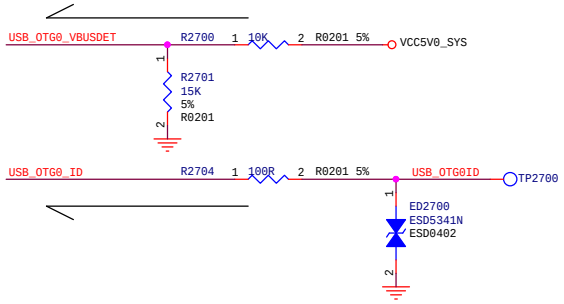


Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_TABLET_REF				
File:	18.Power_DiscretePower				
Date:	Saturday, October 28, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	18 of 27

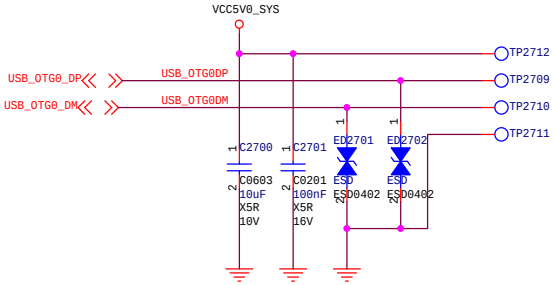


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD			
Project:	RK3566_TABLET_REF		
File:	19.Flash-eMMC_Flash		
Date:	Saturday, October 28, 2023	Rev:	V1.0
Designed by: wu	Reviewed by: CJX	Sheet:	19 of 27

USB2.0 OTG



If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability



Geniatech 深圳金亞太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	20.USB2/USB3_Port				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	20 of 27

RGMII TO RJ45

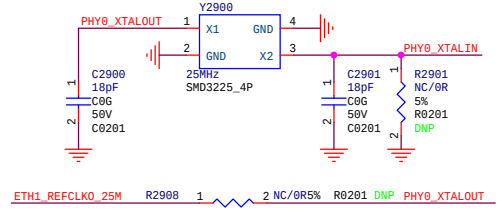
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK

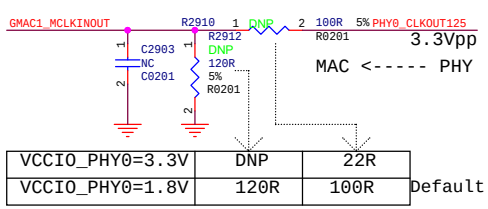
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS

GMAC1_RXCLK
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO

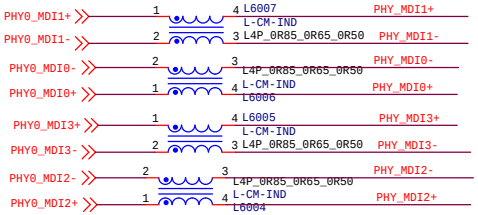
GMAC1_RSTn

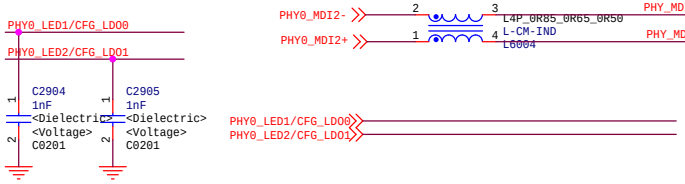
GMAC1_INT/PMEB



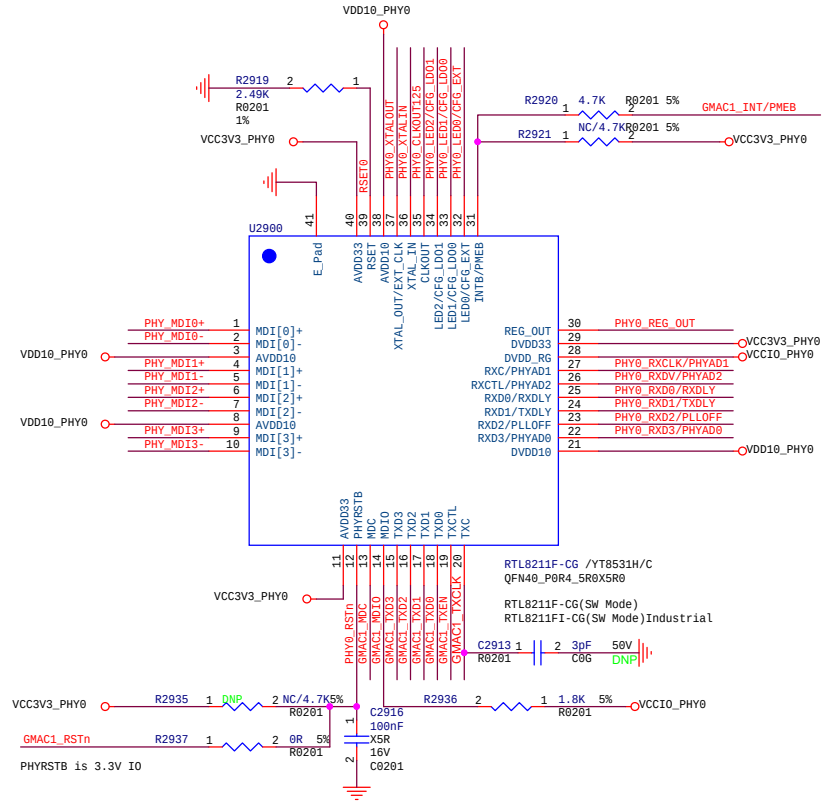


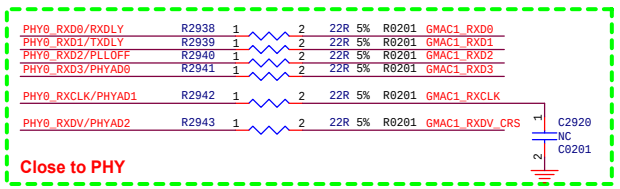
VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

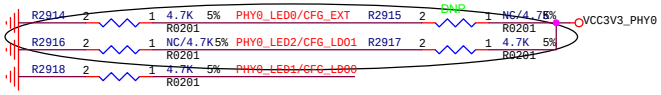




Reserve for EMI.

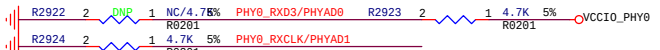






VCC_PHY0_IO Voltage Config

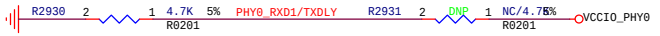
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	



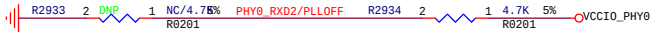
PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

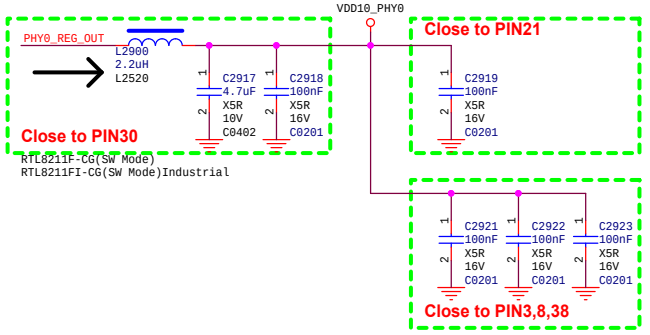
Pull-up for additional 2ns delay to RXC for data latching

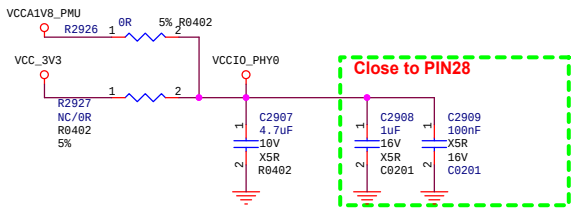


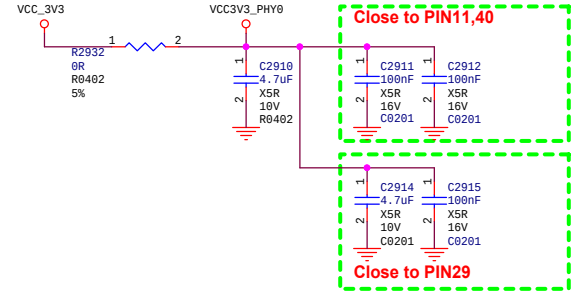
Pull-up for additional 2ns delay to TXC for data latching



Pull-up to disable PLL @ ALDPS mode(Low power mode)

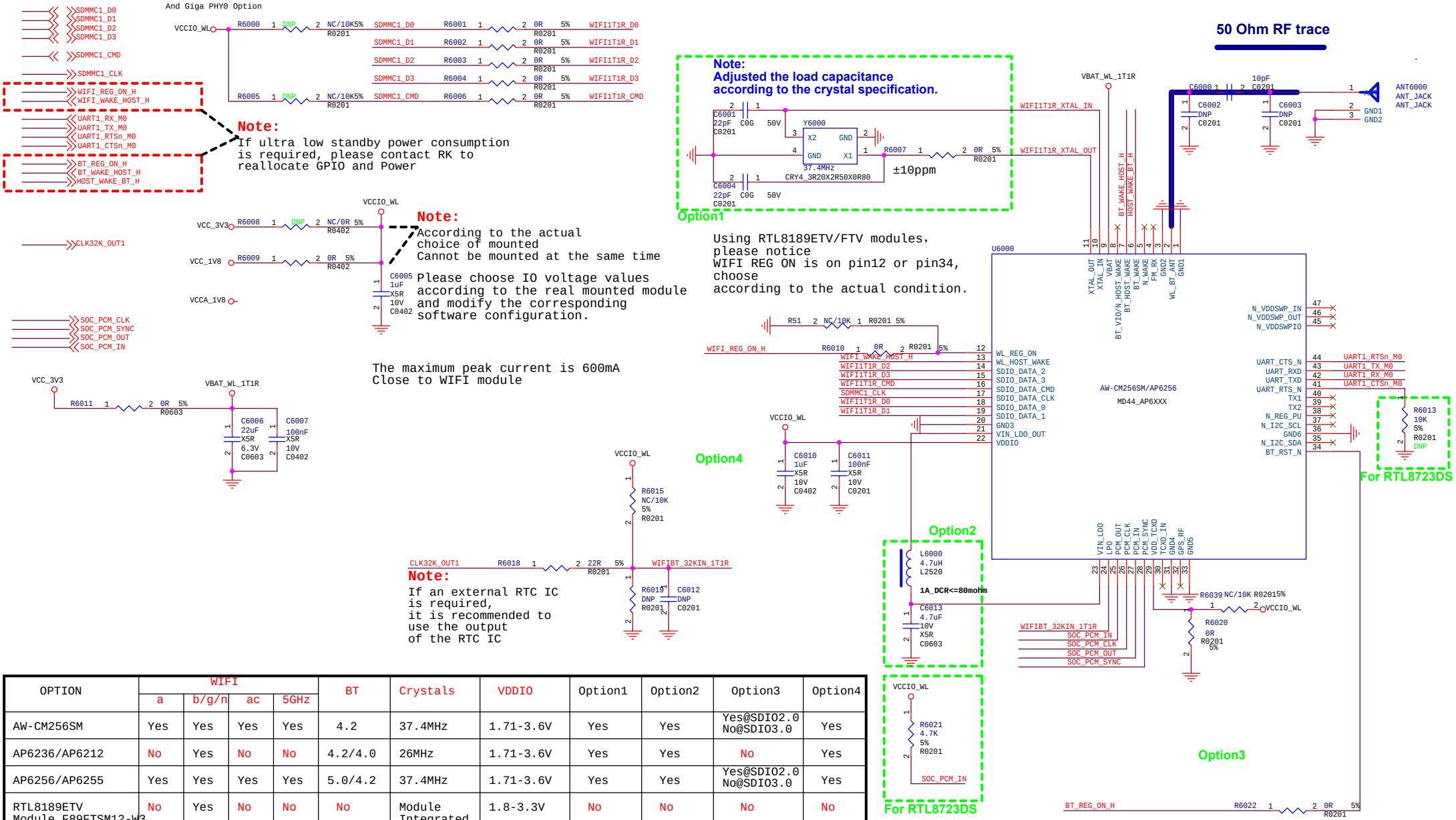






Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD				
Project:	RK3566_TABLET_REF				
File:	28.Ethernet-GPHY_RGMII1				
Date:	Thursday, December 14, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	cjx	Sheet:	21 of 27

SDIO WIFI/BT MODULE



OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

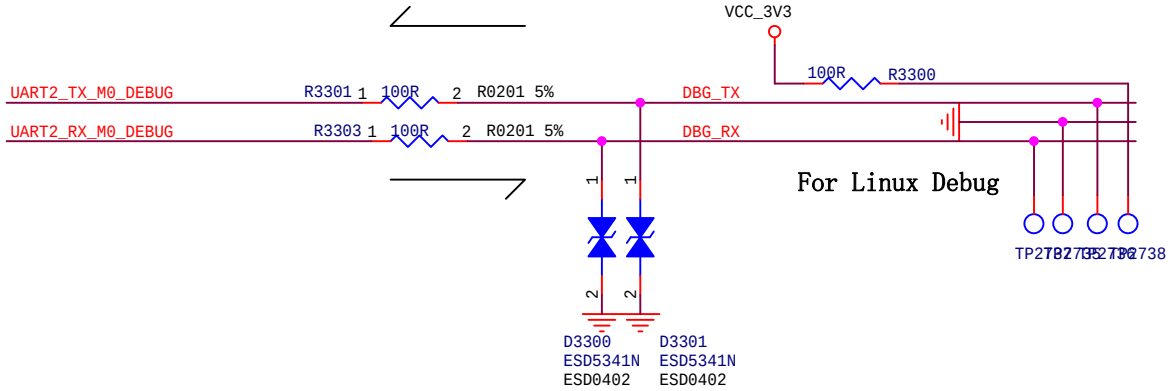
Geniatech	深圳金亚大科技有限公司 SHENZHEN GENIATECH INC., LTD
Project:	RK3566_TABLET_REF
File:	22.WIFI/BT-SDMMC1_1T1R + UART
Date:	Saturday, October 28, 2023
Rev:	V1.0
Designed by:	wu
Reviewed by:	cjx
Sheet:	22 of 27

Geniatech	深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD
Project:	RK3566_TABLET_REF
File:	23.KEY_Array/LED
Date:	Saturday, October 28, 2023
Rev:	V1.0
Designed by:	wu
Reviewed by:	CJX
Sheet:	23 of 27

UART2_RX_M0_DEBUG

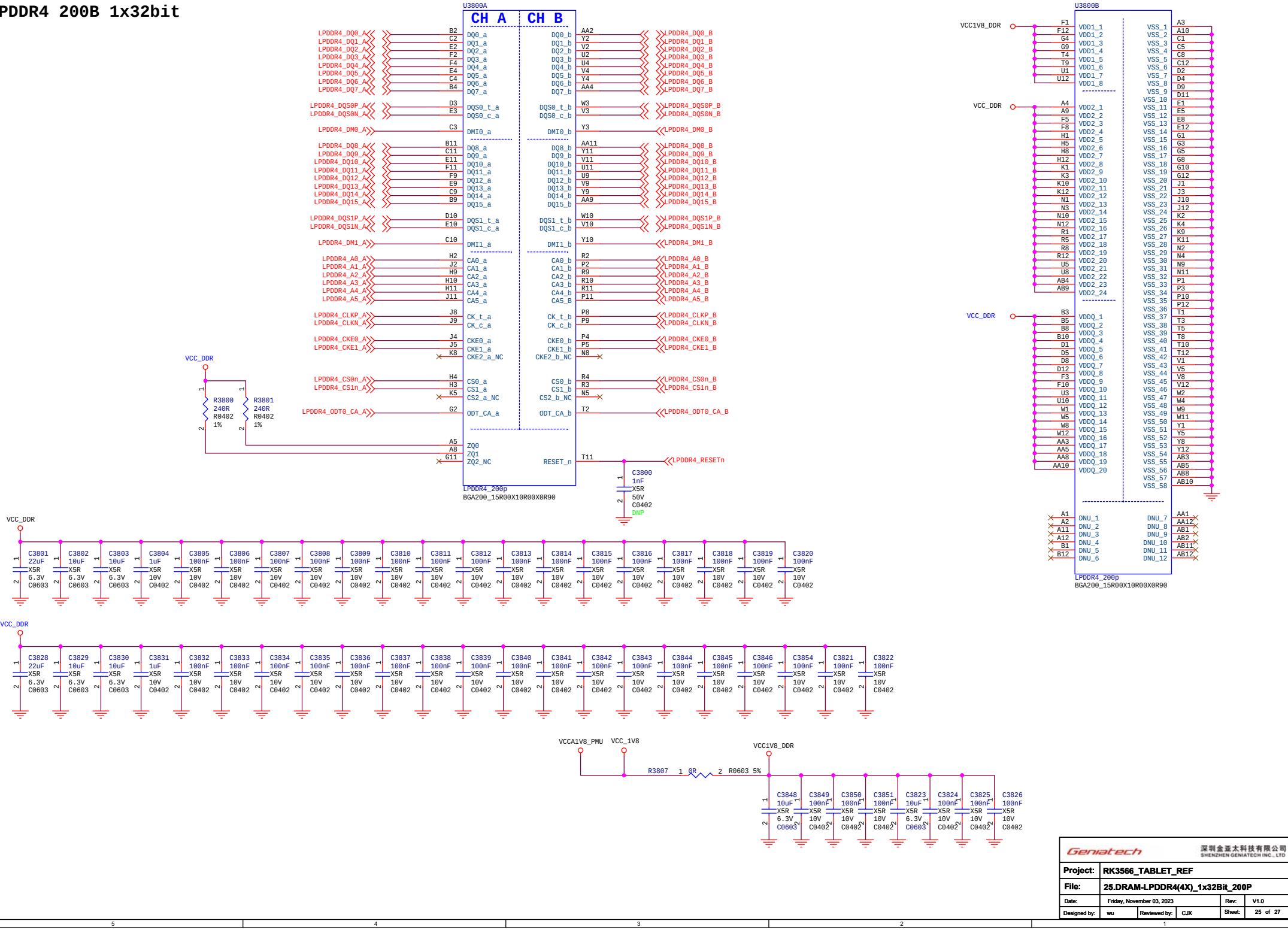
UART2_TX_M0_DEBUG

Debug UART2

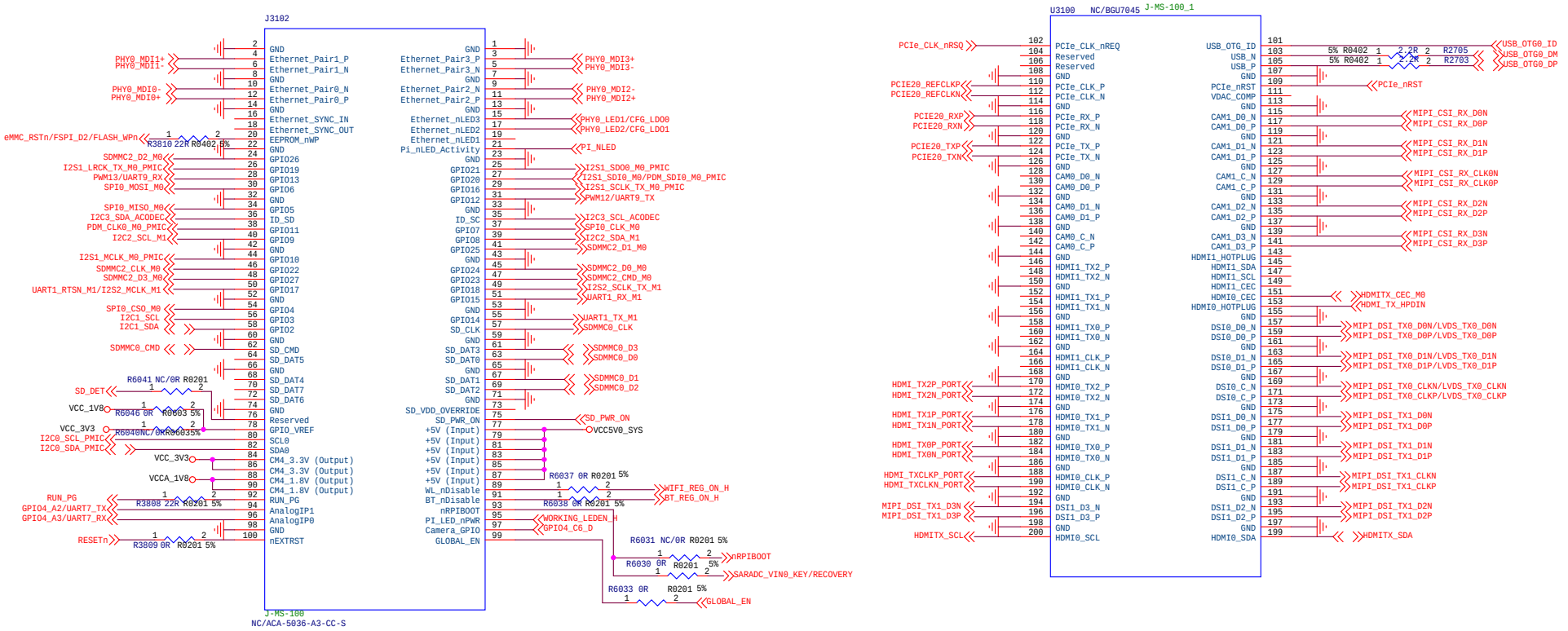


Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	24.Debug_UART/IR				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	24 of 27

LPDDR4 200B 1x32bit



Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	25.DRAM-LPDDR4(4X)_1x32Bit_200P				
Date:	Friday, November 03, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	25 of 27

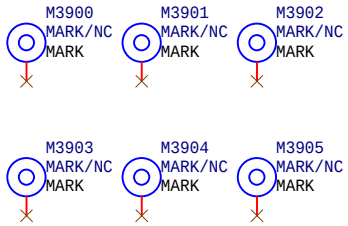


升级按键，音频接口，电源，复位，串口 USB_DET SD_DET

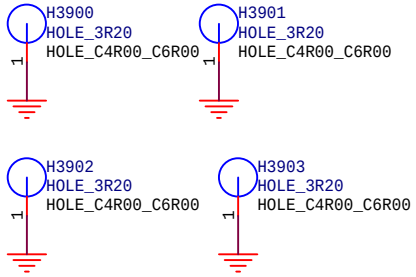
Project:	RK3566_TABLET_REF		
File:	34.BTB Connector(Main)		
Date:	Thursday, December 14, 2023	Rev:	V1.0
Designed by:	wu	Reviewed by: cjx	Sheet: 26 of 27

Page of Accessories

PCB Mark Point



Mechanical Hole



Heatsink

Geniatech 深圳金亚太科技有限公司 SHENZHEN GENIATECH INC., LTD					
Project:	RK3566_TABLET_REF				
File:	27.Mark/Hole/Heatsink				
Date:	Saturday, October 28, 2023			Rev:	V1.0
Designed by:	wu	Reviewed by:	CJX	Sheet:	27 of 27