OSMG2L Industrial Core Board Hardware Manual

Revision History

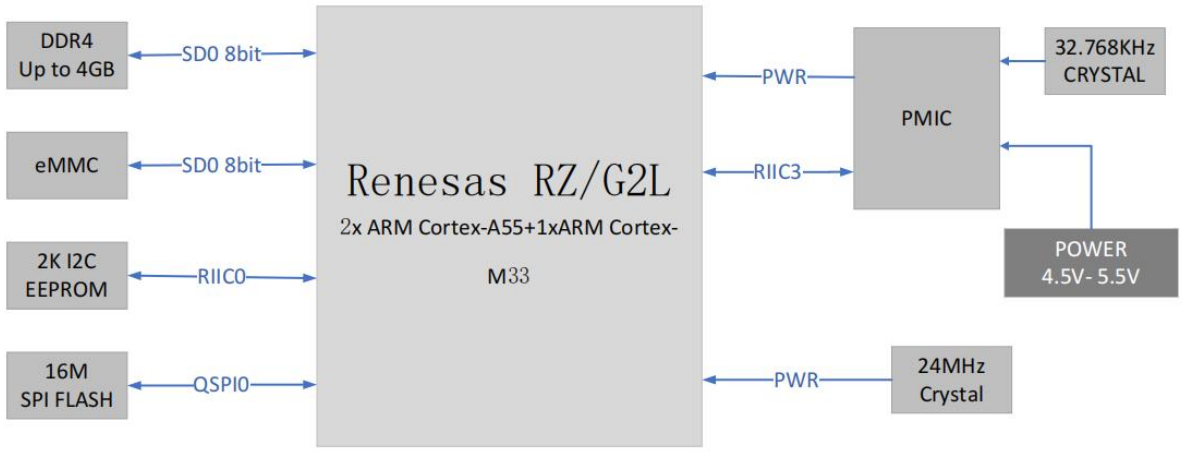
Draft Date	Revision No.	Description
2023/09/23	V1.0	Initial Release
2023/10/09	V1.01	Modify the pin pull-up parameters in section 2.4
2023/10/13	V1.02	Delete the F21 pin pull-up in section 2.4

CONTENTS

1 Product Description

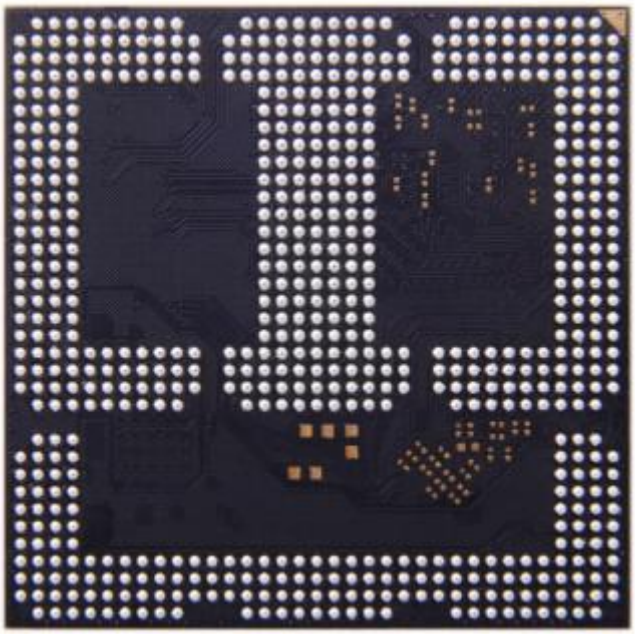
OSM_G2L core board adopts a high-density and high-speed board design, integrating hardware resources such as RZ/G2L, DDR4, eMMC, E2PROM, SPI Flash, PMIC power management and other hardware resources on a board with the size of 45mm*45mm, as well as eliciting IOs through the definition of the non-standard OSM_V1.1.

Note: This core board references the OSM-L standard for IO pinout, LGA package, but some IO levels are different from the OSM standard.



Hardware Block Diagram of Core Board

Front view of core board

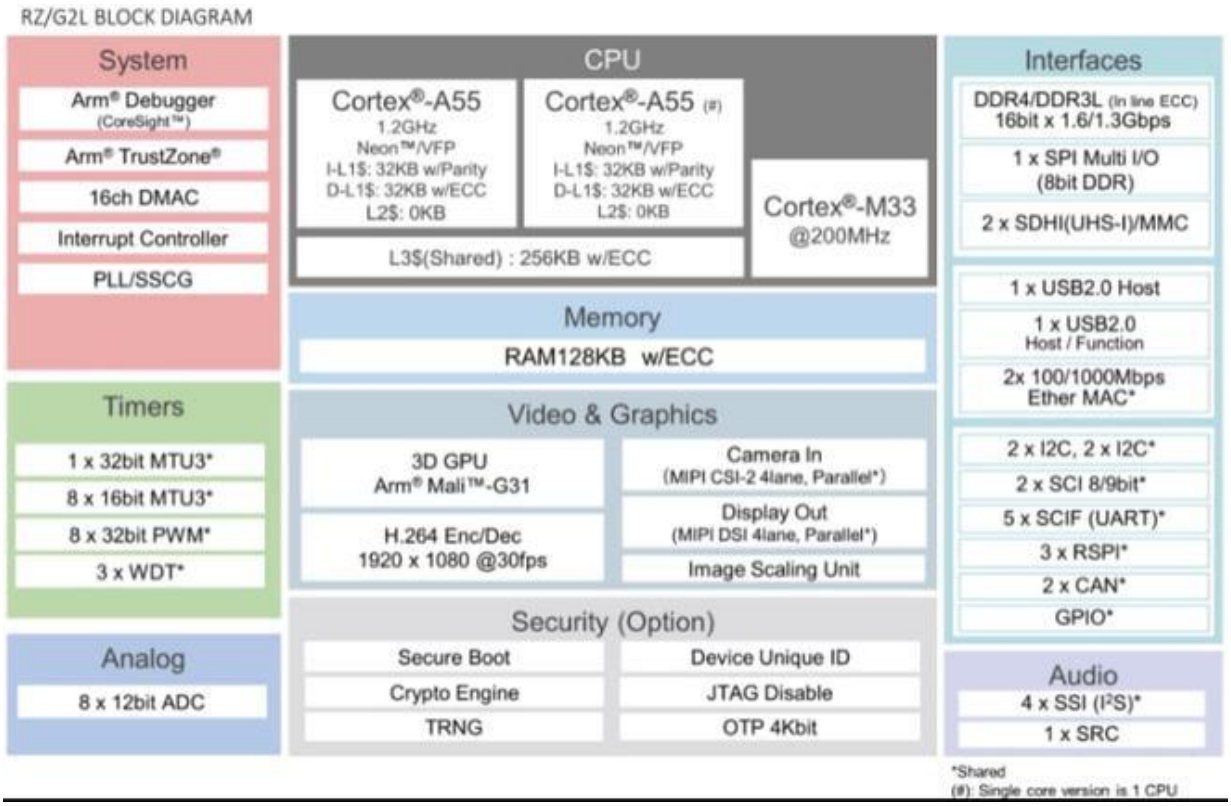


Back view of the core board

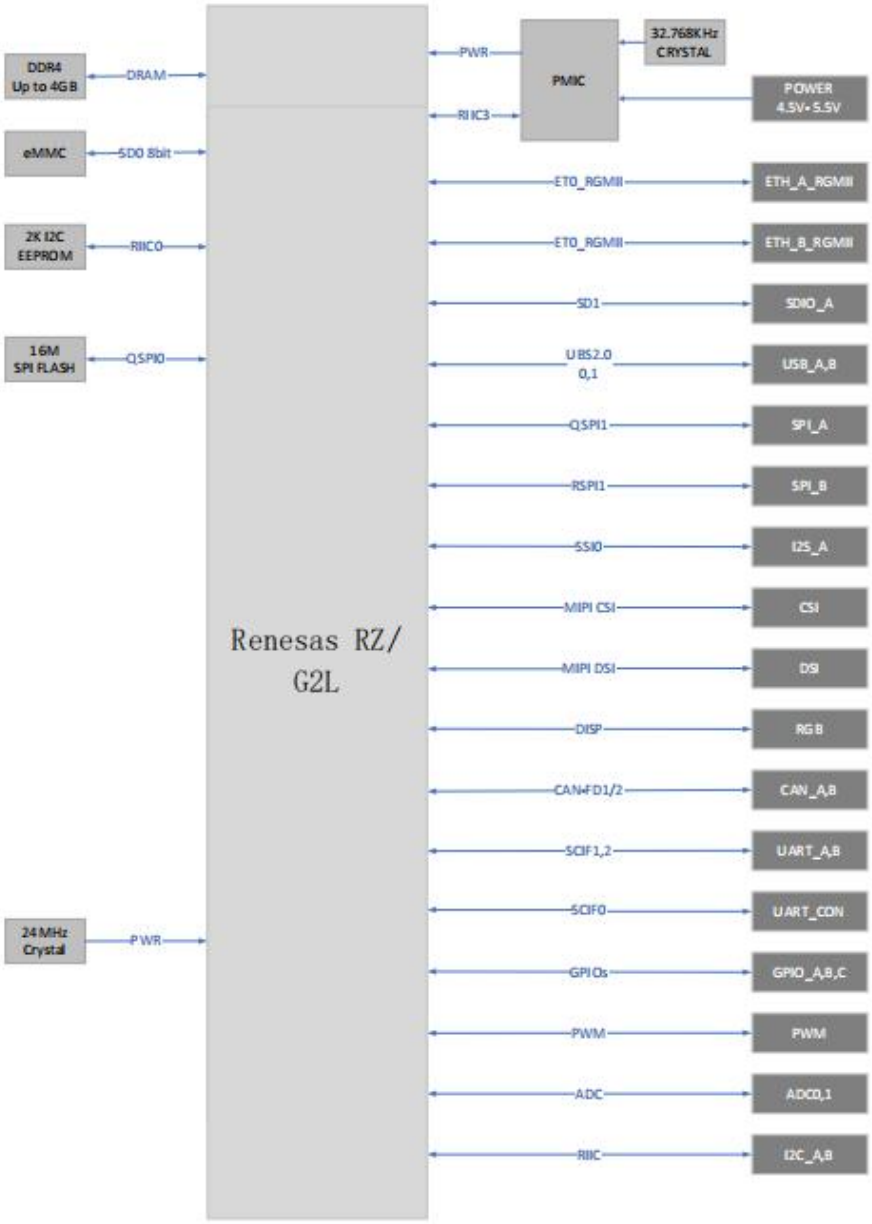
1.1 CPU

Core board CPU model is R9A07G044L23GBG, LFBGA package, 456 pins, size 15mm*15mm, operating temperature range is -40℃~+85℃.

Renesas RZ/G2L processor architecture is as follows:



Renesas RZ/G2L	Dual ARM Cortex-A55，Main frequency 1.2GHz，Support floating point function
	ARM Cortex-M33 dedicated real-time processing unit with 200MHz main frequency
	VPU： Encoding / Decoding support H.264 / AVC (High Profile / Main Profile / Baseline Profile)，H.264 / MVC (Stereo High Profile)，Maximum pixel rate: 1920 x 1080 x@30 fps
	GPU：Mali-G31 500MHz，support OpenGL ES 1.1/2.0/3.1/3.2、Vulkan 1.1、OpenCL 2.0
	ISU：Maximum input image resolution: 5M (2800×2047)，Maximum output image resolution: Full HD (1920 × 1080) with color format conversion support - RGB / ARGB / YcbCr422 / YcbCr420 / RAW(Grayscale)



Renesas RZ/G2LProcessor Function Block Diagram

1.2 ROM

Core board connects to an eMMC chip via the SDHI0 bus of the CPU, using an 8-bit data line compatible with the following eMMC configurations.

Vendor	Model	Size	Operating temperature
Longsys	FEMDRW016G-88A43	16GByte	Industrial grade (-40~85℃)
	FEMDRW032G-88A19	32GByte	Industrial grade (-40~85℃)
SANDISK)	SDINBDG4-16G-XI1	16GByte	Industrial grade (-40~85℃)

1.3 RAM

Core board connects one DDR4 chip through the CPU's dedicated DRAM bus, using a 16-bit data line.DDR4-compatible models are listed in the table below, and support DDR4- 1600 operating mode (800MHz).

Vendor	Model	Size	Operating temperature
Nanya	NT5AD512M16C4-JRI	1GByte	Industrial grade(-40~85℃)
Micron	MT40A512M16LY-062E IT	1GByte	Industrial grade(-40~85℃)
	MT40A1G16KD-062E:E	2GByte	Industrial grade(-40~85℃)

1.4 Crystal oscillator

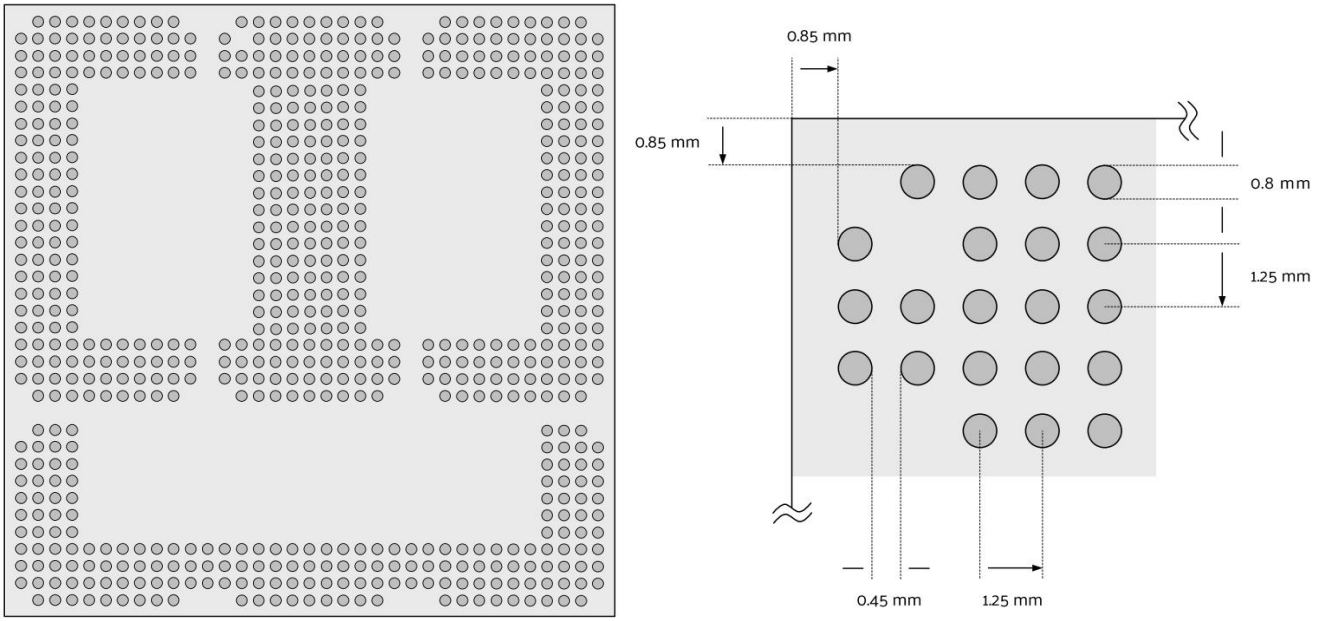
Core board adopts two industrial-grade crystals Y1 and Y2, of which Y1 clock frequency is 32.768KHz, providing a clock source for the PMIC internal RTC; Y2 clock frequency is 24MHz, providing a clock source for the clock chip; and the clock chip then provides a system clock source for the CPU, CAM, I2S, and AUDIO, etc. respectively.

1.5 Power supply

Core board is designed with an industrial-grade PMIC power management chip to meet the system's power supply requirements and CPU power-up and power-down timing requirements, and is powered by a 5.0V DC power supply

1.6 LGA Package

Core board is packaged in an LGA package with 662pins and 1.25mm pitch.



SOM G2L LGA package diagram

1.7 External Interface Resources

The main external interface resources and performance parameters of the core board leading to the CPU are shown in the following table.

External Interface	Quantities	Performance Parameters
MIPI CSI	1	Provides a 4-lane MIPI camera serial interface, supports up to 1.5Gbps per lane, Support 5MP, 30 fps (RAW12)
MIPI DSI	1	Provides 1 4-lane MIPI display serial interface, supporting up to 1.5 Gbps per lane; supports up to resolution is 1920 x 1080@60fps(RGB888);
USB HOST	1	Compliance with USB2.0（supports up to 480 Mbps）;
USB OTG	1	Compliance with USB2.0（supports up to 480 Mbps）; Supports On-The-Go (OTG) Function
DVP	1	Supports WXGA((1280 × 800)60 fps Support Output Data Format: RGB666 / RGB888 CLK / HD / VD timing signal supported
Ethernet	2	Includes 1x ENET, 1x ENET_QOS network port; Supports RMII/RGMII interfaces, where RMII supports 1.8V/3.3V levels and RGMII supports 1.8V/3.3V Power Levels;

		Supports 10/100/1000Mbps network port configuration; Supports network adaption;
SD	2	Supports 1-bit / 4-bit SD bus Channel 0 supports SDHI / e-MMC (boot supported) Channel 1 supports SDHI Compliant with SD 3.0 Supports default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported
CAN FD	2	Compliant with CAN-FD ISO 11898-1 (CD2014) with transmission speeds up to 4Mbps
SPI	1	Supports master and slave modes Programmable bit length, clock polarity, clock phase selectable Maximum transmission rate is: 50 Mbps
UART	4	The maximum supported baud rate is 5Mbps; Supports hardware or software flow control;
I2C	3	Supports master and slave modes, multi-host operation, and timeout detection Supports 7bit and 10bit slave address formats; Note: The core board's onboard EEPROM has used I2C0 at address 0x50.
PWM	1	Has a 16-bit time base counter; Supports up to 66MHz operating frequency;
Watchdog	3	Watchdog Timer; Supports time setting range of 0.5~128s; The time resolution is 0.5s
Audio	1	Supports I2S, Mono, and TDM modes;
QSPI	1	Maximum Clock Frequency: 50 MHz (Quad-SPI DDR), 66 MHz (Quad SPI SDR),100 MHz (Octal-SPI, HyperFlash)
ADC	2	Resolution is: 12-bit Input voltage: 0V~1.8V Conversion time: 1us Operation mode: single scan/continuous scan A/D conversion start condition: - Software trigger - Asynchronous trigger (support external

		trigger) - Synchronous trigger The timers are issued (MTU and PWM timers.);
JTAG	1	Supports JTAG debugging interface

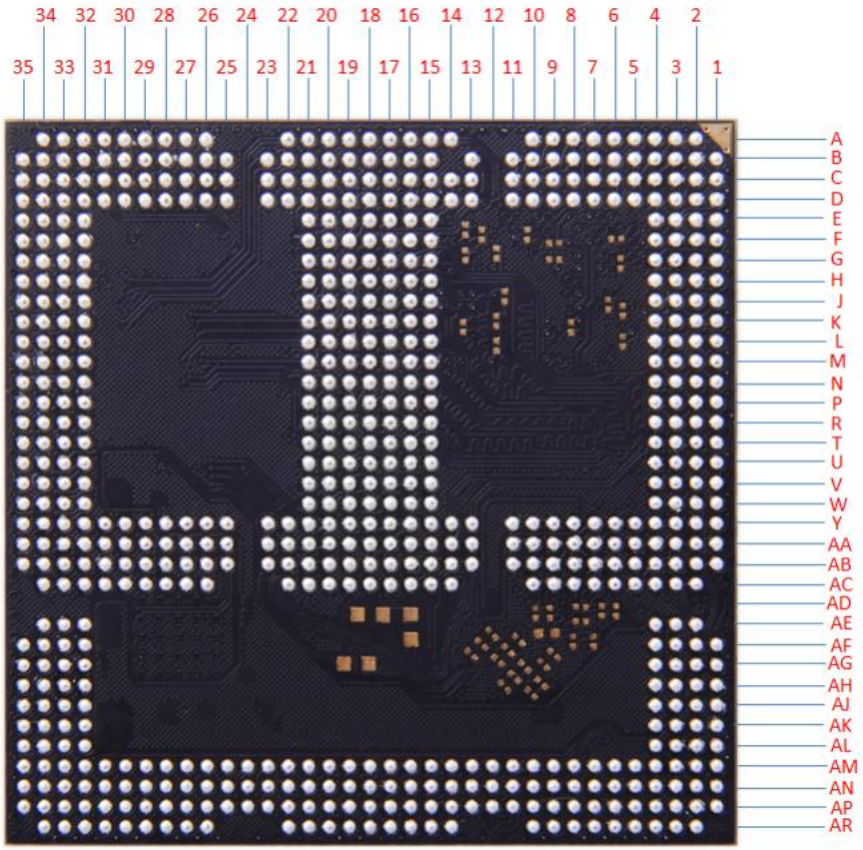
Some of the peripheral resources exist in the case of pin multiplexing, in the actual development process, you can refer to the product information provided by our company "OSM_G2L_ Pin_list_V2.0 Functional Definition -230926" file for reasonable allocation of peripheral resources.

Some peripheral resources exist pin multiplexing, in the actual development process, please prioritize the use of pin default function, please be careful to modify, otherwise it may conflict with the factory driver, if you need to change, please confirm with our technical staff.

2 Pin Description

2.1 Pin Arrangement

Core board comes in an LGA package and the pinout is shown below.



2.2 Pin Definitions

Core board pins are defined in the following table.

The "Chip Pin No." is the serial number of the CPU pin;

"Chip Pin Name" is the complete pin signal name of the CPU, including all the multiplexed signals;

"Pin Function" is the recommended function description of the core board pins;

"Reference Level" is the core board pin operating level standard. is the recommended function description of the core board pins;

"Reference Level" is the core board pin operating level standard.

"-" for "Chip Pin No." means that the pin signal is not connected to the CPU pin.

Pin No.	G2L Chip Pin No.	G2L Chip Pin Name	Pin Default Function	Level	Instruction
A2	AH12	CSI_DATA1_N	CSI_DATA1_N		
A3	AJ12	CSI_DATA1_P	CSI_DATA1_P		
A5	AH14	CSI_DATA2_N	CSI_DATA2_N		
A6	AJ14	CSI_DATA2_P	CSI_DATA2_P		
B1	AJ13	CSI_DATA0_P	CSI_DATA0_P		
B3	AG12	CSI_CLKN	CSI_CLKN		
B4	AG13	CSI_CLKP	CSI_CLKP		
B6	AH11	CSI_DATA3_N	CSI_DATA3_N		
B7	AJ11	CSI_DATA3_P	CSI_DATA3_P		
C1	AH13	CSI_DATA0_N	CSI_DATA0_N		
C2	/	5P35023B-629NLGI(PIN19)	CAM_MCLK	1.8V	
A14	B17	P40_1	SCIF1_RXD	3.3V	
B13	C17	P40_1	SCIF1_TXD	3.3V	
C13	A18	P41_1	SCIF1_RTS	3.3V	
C14	E17	P41_0	SCIF1_CTS	3.3V	
D13	B22	P48_0	SCIF2_TXD	3.3V	
D14	A23	P48_1	SCIF2_RXD	3.3V	

D15	C22	P48_4	SCIF2_RTS	3.3V	
D16	B23	P48_3	SCIF2_CTS	3.3V	
D22	B15	P38_1	SCIF0_RXD	3.3V	
D23	A15	P38_0	SCIF0_TXD	3.3V	
AC18	AE18	DEBUG_EN	DEBUG_EN	3.3V	
D3	AJ24	P15_1	RZ_P15_1	3.3V	
D4	AH24	P16_0	RZ_P16_0	3.3V	
D17	A11	P0_0	RZ_P0_0	3.3V	
D19	AJ3	P42_2	RZ_P42_2	3.3V	
E3	AJ25	P16_1	RZ_P16_1	3.3V	
E4	AH25	P17_0	RZ_P17_0	3.3V	
E17	B12	P0_1	RZ_P0_1	3.3V	
E18	R3	P28_1	PWM_0	3.3V	
E19	B18	P43_0	RZ_P43_0	3.3V	
F3	A26	P17_1	RZ_P17_1	3.3V	
F4	AH26	P17_2	RZ_P17_2	3.3V	
F17	C13	P1_0	RZ_P1_0	3.3V	
F19	D17	P43_1	RZ_P43_1	3.3V	
G3	B13	P2_0	RZ_P2_0	3.3V	
G4	A17	P40_2	RZ_P40_2	3.3V	
G17	A12	P1_1	RZ_P1_1	3.3V	
G19	E18	P43_2	RZ_P43_2	3.3V	
H17	A13	P2_1	RZ_P2_1	3.3V	
H19	C18	P43_3	RZ_P43_3	3.3V	
J17	A14	P3_0	RZ_P3_0	3.3V	
J19	B20	P47_0	RZ_P47_0	3.3V	
K17	B14	P3_1	RZ_P3_1	3.3V	
K19	A20	P47_1	RZ_P47_1	3.3V	

L17	AH16	P4_1	RZ_P4_1	3.3V	
L19	A21	P47_2	RZ_P47_2	3.3V	
B29	/	/	VREF_DDR	0.6V	
C5	/	/	VTTREF_DDR	0.6V	
C20	/	RAA215300(PIN35)LDO_OUT	VDD_SD1_M	3.3V	
M19	/	/	D1.8V_M	1.8V	
T17	/	MD_BOOT0/MD_BOOT2	FORCE_nRECOVERY	3.3V	
U17	/	RS1G08XF5（PIN1）	SYS_RESET	3.3V	
V17	/	RAA215300(PIN55)MPIO1/VR_E	PMIC_EXT_EN	3.3V	
W17	/	RAA215300(PIN30)VBAT	VBAT_RTC_3V	3.0V	
Y3	/	/	D3.3V_M	3.3V	
Y8	/	/	VCC5V0_SYS	5V	
Y9	/	/	VCC5V0_SYS	5V	
Y10	/	/	VCC5V0_SYS	5V	
Y11	/	/	VCC5V0_SYS	5V	
Y16	/	/	D1.2V_M	1.2V	
Y17	/	/	VCC5V0_SYS	5V	
Y20	/	/	D1.1V_M	1.1V	
Y25	/	/	VCC5V0_SYS	5V	
Y26	/	/	VCC5V0_SYS	5V	
Y27	/	/	VCC5V0_SYS	5V	
Y28	/	/	VCC5V0_SYS	5V	
AA9	/	RAA215300(PIN52) PWRON	PMIC_PWRON	1.8V--5V	
AA33	/	/	VDD_SD0_M	1.8V/3.3V	
AE4	/	/	VCC5V0_SYS	5V	
AF4	/	/	VCC5V0_SYS	5V	
AG4	/	/	VCC5V0_SYS	5V	
AH3	/	/	VCC5V0_SYS	5V	

AH4	/	/	VCC5V0_SYS	5V	
AJ3	/	/	VCC5V0_SYS	5V	
AJ4	/	/	VCC5V0_SYS	5V	
AK4	/	/	VCC5V0_SYS	5V	
D20	B2	P19_1	SD1_WP	1.8V/3.3V	
D21	B16	P39_2	SD1_PWER_EN	1.8V/3.3V	
E20	J2	SD1_CMD	SD1_CMD	1.8V/3.3V	
F21	H3	SD1_CLK	SD1_CLK	1.8V/3.3V	
G20	H1	SD1_DATA0	SD1_DATA0	1.8V/3.3V	
G21	H2	SD1_DATA1	SD1_DATA1	1.8V/3.3V	
H20	K2	SD1_DATA2	SD1_DATA2	1.8V/3.3V	
H21	J1	SD1_DATA3	SD1_DATA3	1.8V/3.3V	
J21	B1	P19_0	SD1_CD	1.8V/3.3V	
U15	C7	QSPI1_IO0	QSPI1_IO0	3.3V	
U16	B7	QSPI1_SPCLK	QSPI1_SPCLK	3.3V	
V15	D7	QSPI1_IO1	QSPI1_IO1	3.3V	
W15	D8	QSPI1_IO3	QSPI1_IO3	3.3V	
W16	A6	QSPI1_IO2	QSPI1_IO2	3.3V	
Y15	C8	QSPI1_SSL	QSPI1_SSL	3.3V	
Y21	A19	P44_0	RSPI1_CK	3.3V	
Y22	D18	P44_2	RSPI1_MISO	3.3V	
Y23	F17	P44_1	RSPI1_MOSI	3.3V	
AA23	B19	P44_3	RSPI1_SSL	3.3V	
C3	A25	RIIC0_SDA	RIIC0_SDA	3.3V	
C4	B24	RIIC0_SCL	RIIC0_SCL	3.3V	
AA15	C23	RIIC1_SCL	RIIC1_SCL	3.3V	
AA16	A24	RIIC1_SDA	RIIC1_SDA	3.3V	
AA20	A10	P46_1	RIIC2_SCL	3.3V	

AA21	B10	P46_0	RIIC2_SDA	3.3V	
C6	W2	P37_0	ET1_MDC	1.8V/3.3V	
C7	W1	P37_1	ET1_MDIO	1.8V/3.3V	
F1	AA2	P30_1	ET1_TXD1	1.8V/3.3V	
F2	Y2	P31_1	ET1_TXD3	1.8V/3.3V	
G1	AB1	P30_0	ET1_TXD0	1.8V/3.3V	
G2	AA1	P31_0	ET1_TXD2	1.8V/3.3V	
H1	AB2	P29_0	ET1_TXC	1.8V/3.3V	
J1	AC3	P34_1	ET1_RXD0	1.8V/3.3V	
J2	Y1	P29_1	ET1_TX_CTL	1.8V/3.3V	
K1	AC4	P35_0	ET1_RXD1	1.8V/3.3V	
K2	V3	P36_1	ET1_RX_ERR	1.8V/3.3V	
L1	AC2	P34_0	ET1_RX_CTL	1.8V/3.3V	
M1	AB4	P35_1	ET1_RXD2	1.8V/3.3V	
N1	AB3	P36_0	ET1_RXD3	1.8V/3.3V	
P1	AC1	P33_1	ET1_RXC	1.8V/3.3V	
G15	M2	P21_0	ET0_TXD1	1.8V/3.3V	
G16	L2	P22_0	ET0_TXD3	1.8V/3.3V	
H15	M1	P20_2	ET0_TXD0	1.8V/3.3V	
H16	L1	P21_1	ET0_TXD2	1.8V/3.3V	
J15	N1	P20_0	ET0_TXC	1.8V/3.3V	
K15	R2	P25_0	ET0_RXD0	1.8V/3.3V	
K16	N2	P20_1	ET0_TX_CTL	1.8V/3.3V	
L15	R1	P25_1	ET0_RXD1	1.8V/3.3V	
L16	N3	P27_0	ET0_RX_ERR	1.8V/3.3V	
M15	P1	P24_1	ET0_RX_CTL	1.8V/3.3V	
M17	N6	ETHER0_PVDD	ETHER_IO_VDD	1.8V/3.3V	
T15	U1	P28_0	ET0_MDIO	1.8V/3.3V	

T16	U2	P27_1	ET0_MDC	1.8V/3.3V	
N15	T2	P26_0	ET0_RXD2	1.8V/3.3V	
P15	T1	P26_1	ET0_RXD3	1.8V/3.3V	
R15	P2	P24_0	ET0_RXC	1.8V/3.3V	
J3	A22	P48_2	DISP_nRST(RGB_RESET)	3.3V	
J4	AH28	P7_1	DISP_DE(RGB_DE)	3.3V	
K3	AH27	P6_1	DISP_HSYNC(RGB_HSYNC)	3.3V	
K4	B21	P47_3	DISP_PWREN(RGB_DISP)	3.3V	
L3	AT28	P7_0	DISP_VSYNC(RGB_VSYNC)	3.3V	
M3	AH23	P15_0	DISP_DATA17(RGB_B5)	3.3V	
M4	AJ27	P6_0	DISP_CLK(RGB_CLK)	3.3V	
N3	AG27	P14_0	DISP_DATA15(RGB_B3)	3.3V	
N4	AJ23	P14_1	DISP_DATA16(RGB_B4)	3.3V	
P3	AG26	P13_2	DISP_DATA14(RGB_B2)	3.3V	
R3	AG23	P13_1	DISP_DATA13(RGB_B1)	3.3V	
R4	AF23	P13_0	DISP_DATA12(RGB_B0)	3.3V	
T3	AE22	P12_0	DISP_DATA10(RGB_G4)	3.3V	
T4	AE23	P12_1	DISP_DATA11(RGB_G5)	3.3V	
U3	AF22	P11_1	DISP_DATA9(RGB_G3)	3.3V	
V3	AH22	P10_1	DISP_DATA7(RGB_G1)	3.3V	
V4	AG22	P11_0	DISP_DATA8(RGB_G2)	3.3V	
W4	AJ22	P10_0	DISP_DATA6(RGB_G0)	3.3V	
Y4	AH21	P9_1	DISP_DATA5(RGB_R5)	3.3V	
Y5	AJ21	P9_0	DISP_DATA4(RGB_R4)	3.3V	
Y6	AJ20	P8_1	DISP_DATA2(RGB_R2)	3.3V	
Y7	AT19	P7_2	DISP_DATA0(RGB_R0)	3.3V	
AA5	AH20	P8_2	DISP_DATA3(RGB_R3)	3.3V	
AA6	AH19	P8_0	DISP_DATA1(RGB_R1)	3.3V	

AB4	AH18	DSI_DATA3_P	DSI_DATA3_P	3.3V	
AB5	AT18	DSI_DATA3_N	DSI_DATA3_N	3.3V	
AB7	AG17	DSI_CLKP	DSI_CLKP	3.3V	
AB8	AG18	DSI_CLKN	DSI_CLKN	3.3V	
AB10	AH16	DSI_DATA0_P	DSI_DATA0_P	3.3V	
AB11	AT16	DSI_DATA0_N	DSI_DATA0_N	3.3V	
AC5	AH15	DSI_DATA2_P	DSI_DATA2_P	3.3V	
AC6	AT15	DSI_DATA2_N	DSI_DATA2_N	3.3V	
AC8	AH17	DSI_DATA1_P	DSI_DATA1_P	3.3V	
AC9	AJ17	DSI_DATA1_N	DSI_DATA1_N	3.3V	
M18	A28	ADC_CH0	ADC_CH0	1.8V	
N18	B28	ADC_CH1	ADC_CH1	1.8V	
N17	AE1	TCK_SWDCLK	TCK_SWDCLK(JTAG_TCK_SWCLK)	1.8V	
N19	AD2	TMS_SWDIO	TMS_SWDIO(JTAG_TMS_SWDIO)	1.8V	
P17	AF1	TD	TDI(JTAG_TDI)	1.8V	
R17	AE2	TDO_SWO	TDO_SWO(JTAG_TDO_SWO)	1.8V	
R19	AF2	TRST_N	TRST_N(JTAG_nTRST)	1.8V	
V18	/	5P35023B-629NLGI(PIN12)	I2S_MCLK	3.3V	
V21	B9	P45_3	I2S0_SDIN	3.3V	
W18	D12	P45_1	I2S0_LRCK	3.3V	
W20	A8	P45_0	I2S0_BCK	3.3V	
W21	A9	P45_2	I2S0_SDOUT	3.3V	
AB13	AT8	USB0_DM	USB0_DM		
AB14	AH4	P5_1	USB0_OTG_ID	3.3V	
AB16	AH10	USB_A_VBUS	USB_A_VBUS	5V	
AC14	AH9	USB0_DP	USB0_DP		
AC15	AJ4	P5_0	USB0_OVRCUR_N	3.3V	
AC16	AJ5	P4_0	USB0_VBUSEN	3.3V	

AB23	AJ7	USB1_DM	USB1_DM		
AC20	AG4	P42_0	USB1_VBUSEN	3.3V	
AC21	AE7	P42_1	USB1_OVRCUR_N	3.3V	
AC22	AH8	USB1_DP	USB1_DP		
AB17	AC5	P42_4	CAN0_RX	3.3V	
AC17	AH3	P42_3	CAN0_TX	3.3V	
AB19	C12	P46_2	CAN1_RX	3.3V	
AC19	D13	P46_3	CAN1_TX	3.3V	
A4	/	/	GND	0V	
A7	/	/	GND	0V	
A10	/	/	GND	0V	
A26	/	/	GND	0V	
A29	/	/	GND	0V	
A32	/	/	GND	0V	
B2	/	/	GND	0V	
B5	/	/	GND	0V	
B8	/	/	GND	0V	
B9	/	/	GND	0V	
B27	/	/	GND	0V	
B28	/	/	GND	0V	
B30	/	/	GND	0V	
B33	/	/	GND	0V	
C11	/	/	GND	0V	
C25	/	/	GND	0V	
C32	/	/	GND	0V	
C35	/	/	GND	0V	
D1	/	/	GND	0V	
D5	/	/	GND	0V	

D8	/	/	GND	0V	
D18	/	/	GND	0V	
D28	/	/	GND	0V	
D34	/	/	GND	0V	
E2	/	/	GND	0V	
E15	/	/	GND	0V	
E21	/	/	GND	0V	
F16	/	/	GND	0V	
F20	/	/	GND	0V	
F33	/	/	GND	0V	
F35	/	/	GND	0V	
G34	/	/	GND	0V	
H2	/	/	GND	0V	
H4	/	/	GND	0V	
H32	/	/	GND	0V	
J16	/	/	GND	0V	
J20	/	/	GND	0V	
J33	/	/	GND	0V	
J35	/	/	GND	0V	
K34	/	/	GND	0V	
L2	/	/	GND	0V	
L4	/	/	GND	0V	
L18	/	/	GND	0V	
M16	/	/	GND	0V	
M20	/	/	GND	0V	
M35	/	/	GND	0V	
N34	/	/	GND	0V	
P2	/	/	GND	0V	

P4	/	/	GND	0V	
P18	/	/	GND	0V	
R1	/	/	GND	0V	
R16	/	/	GND	0V	
R20	/	/	GND	0V	
T34	/	/	GND	0V	
U2	/	/	GND	0V	
U4	/	/	GND	0V	
V1	/	/	GND	0V	
V16	/	/	GND	0V	
V20	/	/	GND	0V	
W3	/	/	GND	0V	
W34	/	/	GND	0V	
Y2	/	/	GND	0V	
Y18	/	/	GND	0V	
AA1	/	/	GND	0V	
AA4	/	/	GND	0V	
AA7	/	/	GND	0V	
AA8	/	/	GND	0V	
AA10	/	/	GND	0V	
AA11	/	/	GND	0V	
AA14	/	/	GND	0V	
AA17	/	/	GND	0V	
AA19	/	/	GND	0V	
AA22	/	/	GND	0V	
AA25	/	/	GND	0V	
AA26	/	/	GND	0V	
AA27	/	/	GND	0V	

AA28	/	/	GND	0V	
AA32	/	/	GND	0V	
AB3	/	/	GND	0V	
AB6	/	/	GND	0V	
AB9	/	/	GND	0V	
AB15	/	/	GND	0V	
AB21	/	/	GND	0V	
AB28	/	/	GND	0V	
AB31	/	/	GND	0V	
AB34	/	/	GND	0V	
AC4	/	/	GND	0V	
AC7	/	/	GND	0V	
AC10	/	/	GND	0V	
AC27	/	/	GND	0V	
AC30	/	/	GND	0V	
AC33	/	/	GND	0V	
AE2	/	/	GND	0V	
AE34	/	/	GND	0V	
AF35	/	/	GND	0V	
AG3	/	/	GND	0V	
AH2	/	/	GND	0V	
AH34	/	/	GND	0V	
AJ35	/	/	GND	0V	
AK3	/	/	GND	0V	
AL2	/	/	GND	0V	
AL34	/	/	GND	0V	
AM13	/	/	GND	0V	
AM16	/	/	GND	0V	

AM19	/	/	GND	0V	
AM22	/	/	GND	0V	
AM35	/	/	GND	0V	
AN3	/	/	GND	0V	
AN6	/	/	GND	0V	
AN9	/	/	GND	0V	
AN11	/	/	GND	0V	
AN15	/	/	GND	0V	
AN18	/	/	GND	0V	
AN21	/	/	GND	0V	
AN33	/	/	GND	0V	
AP2	/	/	GND	0V	
AP5	/	/	GND	0V	
AP8	/	/	GND	0V	
AP13	/	/	GND	0V	
AP16	/	/	GND	0V	
AP19	/	/	GND	0V	
AP22	/	/	GND	0V	
AP25	/	/	GND	0V	
AP28	/	/	GND	0V	
AP31	/	/	GND	0V	
AP34	/	/	GND	0V	
AR14	/	/	GND	0V	
AR17	/	/	GND	0V	
AR20	/	/	GND	0V	
AR26	/	/	GND	0V	
AR29	/	/	GND	0V	
AR32	/	/	GND	0V	

A8	/	/	NC		
A9	/	/	NC		
A15	/	/	NC		
A16	/	/	NC		
A17	/	/	NC		
A18	/	/	NC		
A19	/	/	NC		
A20	/	/	NC		
A21	/	/	NC		
A22	/	/	NC		
A27	/	/	NC		
A28	/	/	NC		
A30	/	/	NC		
A31	/	/	NC		
A33	/	/	NC		
A34	/	/	NC		
B10	/	/	NC		
B11	/	/	NC		
B15	/	/	NC		
B16	/	/	NC		
B17	/	/	NC		
B18	/	/	NC		
B19	/	/	NC		
B20	/	/	NC		
B21	/	/	NC		
B22	/	/	NC		
B23	/	/	NC		
B25	/	/	NC		

B26	/	/	NC		
B31	/	/	NC		
B32	/	/	NC		
B34	/	/	NC		
B35	/	/	NC		
C8	/	/	NC		
C9	/	/	NC		
C10	/	/	NC		
C15	/	/	NC		
C16	/	/	NC		
C17	/	/	NC		
C18	/	/	NC		
C19	/	/	NC		
C21	/	/	NC		
C22	/	/	NC		
C23	/	/	NC		
C26	/	/	NC		
C27	/	/	NC		
C28	/	/	NC		
C29	/	/	NC		
C30	/	/	NC		
C31	/	/	NC		
C33	/	/	NC		
C34	/	/	NC		
D2	/	/	NC		
D6	/	/	NC		
D7	/	/	NC		
D9	/	/	NC		

D10	/	/	NC		
D11	/	/	NC		
D25	/	/	NC		
D26	/	/	NC		
D27	/	/	NC		
D29	/	/	NC		
D30	/	/	NC		
D31	/	/	NC		
D32	/	/	NC		
D33	/	/	NC		
D35	/	/	NC		
E1	/	/	NC		
E16	/	/	NC		
E32	/	/	NC		
E33	/	/	NC		
E34	/	/	NC		
E35	/	/	NC		
F15	/	/	NC		
F18	/	/	NC		
F32	/	/	NC		
F34	/	/	NC		
G18	/	/	NC		
G32	/	/	NC		
G33	/	/	NC		
G35	/	/	NC		
H3	/	/	NC		
H18	/	/	NC		
H33	/	/	NC		

H34	/	/	NC		
H35	/	/	NC		
J18	/	/	NC		
J32	/	/	NC		
J34	/	/	NC		
K18	/	/	NC		
K20	/	/	NC		
K21	/	/	NC		
K32	/	/	NC		
K33	/	/	NC		
K35	/	/	NC		
L20	/	/	NC		
L21	/	/	NC		
L32	/	/	NC		
L33	/	/	NC		
L34	/	/	NC		
L35	/	/	NC		
M2	/	/	NC		
M21	/	/	NC		
M32	/	/	NC		
M33	/	/	NC		
M34	/	/	NC		
N2	/	/	NC		
N16	/	/	NC		
N20	/	/	NC		
N21	/	/	NC		
N32	/	/	NC		
N33	/	/	NC		

N35	/	/	NC		
P16	/	/	NC		
P19	/	/	NC		
P20	/	/	NC		
P21	/	/	NC		
P32	/	/	NC		
P33	/	/	NC		
P34	/	/	NC		
P35	/	/	NC		
R2	/	/	NC		
R18	/	/	NC		
R21	/	/	NC		
R32	/	/	NC		
R33	/	/	NC		
R34	/	/	NC		
R35	/	/	NC		
T1	/	/	NC		
T2	/	/	NC		
T18	/	/	NC		
T19	/	/	NC		
T20	/	/	NC		
T21	/	/	NC		
T32	/	/	NC		
T33	/	/	NC		
T35	/	/	NC		
U1	/	/	NC		
U18	/	/	NC		
U19	/	/	NC		

U20	/	/	NC		
U21	/	/	NC		
U32	/	/	NC		
U33	/	/	NC		
U34	/	/	NC		
U35	/	/	NC		
V2	/	/	NC		
V19	/	/	NC		
V32	/	/	NC		
V33	/	/	NC		
V34	/	/	NC		
V35	/	/	NC		
W1	/	/	NC		
W2	/	/	NC		
W19	/	/	NC		
W32	/	/	NC		
W33	/	/	NC		
W35	/	/	NC		
Y1	/	/	NC		
Y13	/	/	NC		
Y14	/	/	NC		
Y19	/	/	NC		
Y29	/	/	NC		
Y30	/	/	NC		
Y31	/	/	NC		
Y32	/	/	NC		
Y33	/	/	NC		
Y34	/	/	NC		

Y35	/	/	NC		
AA2	/	/	NC		
AA3	/	/	NC		
AA13	/	/	NC		
AA18	/	/	NC		
AA29	/	/	NC		
AA30	/	/	NC		
AA31	/	/	NC		
AA34	/	/	NC		
AA35	/	/	NC		
AB1	/	/	NC		
AB2	/	/	NC		
AB18	/	/	NC		
AB20	/	/	NC		
AB22	/	/	NC		
AB25	/	/	NC		
AB26	/	/	NC		
AB27	/	/	NC		
AB29	/	/	NC		
AB30	/	/	NC		
AB32	/	/	NC		
AB33	/	/	NC		
AB35	/	/	NC		
AC2	/	/	NC		
AC3	/	/	NC		
AC26	/	/	NC		
AC28	/	/	NC		
AC29	/	/	NC		

AC31	/	/	NC		
AC32	/	/	NC		
AC34	/	/	NC		
AE3	/	/	NC		
AE32	/	/	NC		
AE33	/	/	NC		
AF1	/	/	NC		
AF2	/	/	NC		
AF3	/	/	NC		
AF32	/	/	NC		
AF33	/	/	NC		
AF34	/	/	NC		
AG1	/	/	NC		
AG2	/	/	NC		
AG32	/	/	NC		
AG33	/	/	NC		
AG34	/	/	NC		
AG35	/	/	NC		
AH1	/	/	NC		
AH32	/	/	NC		
AH33	/	/	NC		
AH35	/	/	NC		
AJ1	/	/	NC		
AJ2	/	/	NC		
AJ32	/	/	NC		
AJ33	/	/	NC		
AJ34	/	/	NC		
AK1	/	/	NC		

AK2	/	/	NC		
AK32	/	/	NC		
AK33	/	/	NC		
AK34	/	/	NC		
AK35	/	/	NC		
AL1	/	/	NC		
AL3	/	/	NC		
AL4	/	/	NC		
AL32	/	/	NC		
AL33	/	/	NC		
AL35	/	/	NC		
AM1	/	/	NC		
AM2	/	/	NC		
AM3	/	/	NC		
AM4	/	/	NC		
AM5	/	/	NC		
AM6	/	/	NC		
AM7	/	/	NC		
AM8	/	/	NC		
AM9	/	/	NC		
AM10	/	/	NC		
AM11	/	/	NC		
AM12	/	/	NC		
AM14	/	/	NC		
AM15	/	/	NC		
AM17	/	/	NC		
AM18	/	/	NC		
AM20	/	/	NC		

AM21	/	/	NC		
AM23	/	/	NC		
AM24	/	/	NC		
AM25	/	/	NC		
AM26	/	/	NC		
AM27	/	/	NC		
AM28	/	/	NC		
AM29	/	/	NC		
AM30	/	/	NC		
AM31	/	/	NC		
AM32	/	/	NC		
AM33	/	/	NC		
AM34	/	/	NC		
AN1	/	/	NC		
AN2	/	/	NC		
AN4	/	/	NC		
AN5	/	/	NC		
AN7	/	/	NC		
AN8	/	/	NC		
AN10	/	/	NC		
AN12	/	/	NC		
AN13	/	/	NC		
AN14	/	/	NC		
AN16	/	/	NC		
AN17	/	/	NC		
AN19	/	/	NC		
AN20	/	/	NC		
AN22	/	/	NC		

AN23	/	/	NC		
AN24	/	/	NC		
AN25	/	/	NC		
AN26	/	/	NC		
AN27	/	/	NC		
AN28	/	/	NC		
AN29	/	/	NC		
AN30	/	/	NC		
AN31	/	/	NC		
AN32	/	/	NC		
AN34	/	/	NC		
AN35	/	/	NC		
AP1	/	/	NC		
AP3	/	/	NC		
AP4	/	/	NC		
AP6	/	/	NC		
AP7	/	/	NC		
AP9	/	/	NC		
AP10	/	/	NC		
AP11	/	/	NC		
AP12	/	/	NC		
AP14	/	/	NC		
AP15	/	/	NC		
AP17	/	/	NC		
AP18	/	/	NC		
AP20	/	/	NC		
AP21	/	/	NC		
AP23	/	/	NC		

AP24	/	/	NC		
AP26	/	/	NC		
AP27	/	/	NC		
AP29	/	/	NC		
AP30	/	/	NC		
AP32	/	/	NC		
AP33	/	/	NC		
AP35	/	/	NC		
AR2	/	/	NC		
AR3	/	/	NC		
AR4	/	/	NC		
AR5	/	/	NC		
AR6	/	/	NC		
AR7	/	/	NC		
AR8	/	/	NC		
AR9	/	/	NC		
AR10	/	/	NC		
AR15	/	/	NC		
AR16	/	/	NC		
AR18	/	/	NC		
AR19	/	/	NC		
AR21	/	/	NC		
AR22	/	/	NC		
AR27	/	/	NC		
AR28	/	/	NC		
AR30	/	/	NC		
AR31	/	/	NC		
AR33	/	/	NC		

AR34	/	/	NC		

Note: Core board references the OSM-L standard for IO pinout, LGA package, but some IO levels are different from the OSM standard.

2.3 Internal Pin Usage Description

The following table describes the use of the pins inside the core board, "Pin No." is "-" means that the pin is used inside the core board, and not pinned out; otherwise, it means that the core board has been used inside the core board and at the same time pinned out the interface.

Note: Since I2C0 is connected to the core board's EEPROM, it is recommended to avoid slave device address 0x50 when designing the backplane. I2C0,I2C1,I2C2 pull-up resistors to 3.3V on the core board.

OSM Pin No.	**Chip Pin No.**	Chip Pin Name	Pin Default Function	Level
-	F1	SD0_CLK	eMMC	1.8V
-	F2	SD0_CMD	eMMC	1.8V
-	G2	SD0_DATA0	eMMC	1.8V
-	H4	SD0_DATA1	eMMC	1.8V
-	G3	SD0_DATA2	eMMC	1.8V
-	G4	SD0_DATA3	eMMC	1.8V
-	E1	SD0_DATA4	eMMC	1.8V
-	D1	SD0_DATA5	eMMC	1.8V
-	E2	SD0_DATA6	eMMC	1.8V
-	D2	SD0_DATA7	eMMC	1.8V
-	C1	SD0_RST_N	eMMC	1.8V
-	B7	QSPI1_SPCLK	SPI Flash	3.3V
-	C8	QSPI1_SSL	SPI Flash	3.3V
-	C7	QSPI1_IO0	SPI Flash	3.3V
-	D7	QSPI1_IO1	SPI Flash	3.3V
-	A6	QSPI1_IO2	SPI Flash	3.3V

-	D8	QSPI1_IO3	SPI Flash	3.3V
-	AF3	PRST_N	PMIC	3.3V

2.4 Pin pull-up, pull-down, and series description

The following table describes the pins that have been configured with pull-ups and pull downs or series resistors inside the core board. For pins not described in the table, the core board has no pull-up/down configuration by default, and they are directly pinned out.

OSM Pin No.	**Chip Pin No.**	Chip Pin Name	Up/Down Configuration	**Pull-up and pull-down resistor values**
J21	B1	SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA/P19_0	Pull up 3.3V	10K
D20	B2	SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL/P19_1	Pull up3.3V	10K
E20	J2	SD1_CMD	Pull up1.8V/3.3V	10K
G20	H1	SD1_DATA0	Pull up1.8V/3.3V	10K
G21	H2	SD1_DATA1	Pull up1.8V/3.3V	10K
H20	K2	SD1_DATA2	Pull up1.8V/3.3V	10K
H21	J1	SD1_DATA3	Pull up1.8V/3.3V	10K
AB14	AH4	USB0_OTG_ID/SCIF2_CTS/MTIOC7D/SSI2_RCK/P5_1	Pull up 3.3V	10K
AC15	AJ4	USB0_OVRCUR/SCIF2_SCK/MTIOC7C/SSI2_BCK/P5_0	Pull up 3.3V	10K
AC21	AE7	USB1_OVRCUR/RSPI2_MOSI/CAN0_TX/SCIF2_RXD/MTIOC7B/P42_1	Pull up 3.3V	10K
-	AG7	USB_RREF	Pull down GND	1.8K
-	A2	QSPI0_SSL	Pull up 3.3V	10K
-	A3	QSPI0_IO0	Pull up 3.3V	47K
-	B3	QSPI0_IO1	Pull up 3.3V	47K
-	A4	QSPI0_IO2	Pull up 3.3V	47K
-	B4	QSPI0_IO3	Pull up 3.3V	47K
K16	N2	ET0_TX_CTL_TX_EN/RSPI0_MOSI/CAN0_TX/P20_1	series	22R

J15	N1	ET0_TXC_TX_CLK/RSPI0_CK/CAN_CLK/P20_0	series	22R
H15	M1	ET0_TXD0/RSPI0_MISO/CAN0_RX/P20_2	series	22R
G15	M2	ET0_TXD1/RSPI0_SSL/CAN0_TX_DATARATE_EN/P21_0	series	22R
H16	L1	ET0_TXD2/CAN0_RX_DATARATE_EN/P21_1	series	22R
G16	L2	ET0_TXD3/SSI0_BCK/CAN1_TX/MTCLKA/P22_0	series	22R
J2	Y1	ET1_TX_CTL_TX_EN/CAM_HREF/USB1_OVRCUR/SSI2_RCK/P29_1	series	22R
H1	AB2	ET1_TXC_TX_CLK/CAM_PCLK/USB1_VBUSEN/SSI2_BCK/P29_0	series	22R
G1	AB1	ET1_TXD0/CAM_VSYNC/SSI2_DATA/P30_0	series	22R
F1	AA2	ET1_TXD1/CAM_DATA15/P30_1	series	22R
G2	AA1	ET1_TXD2/CAM_DATA0/SCI1_RXD/SSI3_BCK/P31_0	series	22R
F2	Y2	ET1_TXD3/CAM_DATA1/SCI1_TXD/SSI3_RCK/P31_1	series	22R
-	E8	MD_BOOT0	Pull up3.3V	10K
-	E7	MD_BOOT1	Pull down GND	10K
-	G7	MD_BOOT2	Pull up3.3V	10K
-	D23	MD_CLKS	Pull up3.3V	10K
-	E23	MD_OSCDRV0	Pull down GND	10K
-	D27	MD_OSCDRV1	Pull down GND	10K
-	AJ2	NMI	Pull up 3.3V	10K
-	AB23	BSCANP	Pull down GND	10K
-	AB24	CPUHOLD	Pull down GND	10K
-	AD18	TESTMD	Pull down GND	10K
AC18	AE18	DEBUG_EN	Pull up 3.3V	10K
N17	AE1	TCK_SWDCLK	Pull up 1.8V	4.7K
N19	AD2	TMS_SWDIO	Pull up 1.8V	10K
P17	AF1	TDI	Pull up 1.8V	10K

R19	AF2	TRST_N	Pull up 1.8V	1K
AA15	C23	RIIC1_SCL	Pull up 3.3V	2K2
AA16	A24	RIIC1_SDA	Pull up 3.3V	2K2
AA20	A10	P46_1/SSI1_RCK/GTETRGB/CAN1_RX/RIIC2_SCL	Pull up 3.3V	2K2
AA21	B10	P46_0/SSI1_BCK/GTETRGA/CAN1_TX/RIIC2_SDA	Pull up 3.3V	2K2
C3	A25	RIIC0_SDA	Pull up 3.3V	2K2
C4	B24	RIIC0_SCL	Pull up 3.3V	2K2
U17	RS1G08XF5（PIN1）	SYS_RST#	Pull up 3.3V	10K
V17	RAA215300(PIN55)MPIO1/VR_E	CARRIER_PWR_EN	Pull up 3.3V	10K
AA9	RAA215300(PIN52)PWRON	PWR_BTN#	Pull up 1.8V to 5V	10K
T17	-	MD_BOOT0/MD_BOOT2	Pull up 3.3v	10K

2.5 Function Pin Signal Alignment Length and Impedance Description

The following table describes the PCB trace length and impedance of uSDHC, USB, RGMII, MIPI CSI, MIPI DSI, I2S and other function pins inside the core board. The "length of alignment" includes PIN DELAY.

OSM Pin No.	Chip Pin No.	Chip Pin Name	Pin Default Function	Alignment length Degree/mil	Impedance Description
K16	N2	ET0_TX_CTL_TX_EN/RSPI0_MOSI/CAN0_TX/P20_1	ET0_RGMII	2776.54	Single-ended 50ohm
J15	N1	ET0_TXC_TX_CLK/RSPI0_CK/CAN_CLK/P20_0	ET0_RGMII	2461.32	Single-ended 50ohm
H15	M1	ET0_TXD0/RSPI0_MISO/CAN	ET0_RGMII	2615.36	Single-ended

		0_RX/P20_2			50ohm
G15	M2	ET0_TXD1/RSPI0_SSL/CAN0_TX_DATARATE_EN/P21_0	ET0_RGMII	2593.50	Single-ended 50ohm
H16	L1	ET0_TXD2/CAN0_RX_DATARATE_EN/P21_1	ET0_RGMII	2683.45	Single-ended 50ohm
G16	L2	ET0_TXD3/SSI0_BCK/CAN1_TX/MTCLKA/P22_0	ET0_RGMII	2561.83	Single-ended 50ohm
M15	P1	ET0_RX_CTL_RX_DV/SSI1_RCK/POE4_N/P24_1	ET0_RGMII	2059.52	Single-ended 50ohm
L16	N3	ET0_RX_ERR/RSPI1_MISO/MTIOC8C/P27_0/	ET0_RGMII	1665.22	Single-ended 50ohm
R1	P2	ET0_RXC_RX_CLK/SSI1_BCK/POE0_N/P24_0	ET0_RGMII	1785.2	Single-ended 50ohm
K15	R2	ET0_RXD0/SSI1_TXD/POE8_N/P25_0	ET0_RGMII	2140.52	Single-ended 50ohm
R1	L15	ET0_RXD1/SSI1_RXD/POE10_N/P25_1	ET0_RGMII	2086.64	Single-ended 50ohm
N15	T2	ET0_RXD2/RSPI1_CK/MTIOC8A/P26_0	ET0_RGMII	2184.36	Single-ended 50ohm
P15	T1	ET0_RXD3/RSPI1_MOSI/MTIOC8B/P26_1	ET0_RGMII	2109.87	Single-ended 50ohm
F21	H3	SD1_CLK	uSDHC1	2997.85	Single-ended 50ohm
E20	J2	SD1_CMD	uSDHC1	3148.22	Single-ended 50ohm
G20	H1	SD1_DATA0	uSDHC1	3107.31	Single-ended 50ohm
G21	H2	SD1_DATA1	uSDHC1	2857.88	Single-ended

					50ohm
H20	K2	SD1_DATA2	uSDHC1	2977.09	Single-ended 50ohm
H21	J1	SD1_DATA3	uSDHC1	2919.58	Single-ended 50ohm
AB13	AJ8	USB0_DM	USB0	223.63	Increment 90ohm
AC14	AH9	USB0_DP	USB0	225.15	
AJ7	AB23	USB1_DM	USB1	656.00	Increment 90ohm
AH8	AC22	USB1_DP	USB1	658.27	
J2	Y1	ET1_TX_CTL_TX_EN/CAM_HREF/USB1_OVRCUR/SSI2_RCK/P29_1	ET1_RGMII	1914.41	Single-ended 50ohm
H1	AB2	ET1_TXC_TX_CLK/CAM_PCLK/USB1_VBUSEN/SSI2_BCK/P29_0	ET1_RGMII	1815.35	Single-ended 50ohm
G1	AB1	ET1_TXD0/CAM_VSYNC/SSI2_DATA/P30_0	ET1_RGMII	1791.36	Single-ended 50ohm
F1	AA2	ET1_TXD1/CAM_DATA15/P30_1	ET1_RGMII	1784.20	Single-ended 50ohm
G2	AA1	ET1_TXD2/CAM_DATA0/SCI1_RXD/SSI3_BCK/P31_0	ET1_RGMII	1906.85	Single-ended 50ohm
F2	Y2	ET1_TXD3/CAM_DATA1/SCI1_TXD/SSI3_RCK/P31_1	ET1_RGMII	1765.71	Single-ended 50ohm
L1	AC2	ET1_RX_CTL_RX_DV/CAM_DATA6/GTIOC3A/MTIOC0A/GTIOC1A/P34_0	ET1_RGMII	1163.15	Single-ended 50ohm
K2	V3	ET1_RX_ERR/CAM_DATA11/SSI0_RXD/MTIOC3D/GTETRG	ET1_RGMII	1168.23	Single-ended 50ohm

		B/P36_1			
P1	AC1	ET1_RXC_RX_CLK/CAM_DATA5/GTIOC2B/SCIF2_RXD/GTIOC0B/P33_1	ET1_RGMII	1160.43	Single-ended 50ohm
J1	AC3	ET1_RXD0/CAM_DATA7/GTIOC3B/MTIOC0B/GTIOC1B/P34_1	ET1_RGMII	1372.73	Single-ended 50ohm
K1	AC4	ET1_RXD1/CAM_DATA8/SSI0_BCK/MTIOC0C/GTIOC2A/P35_0	ET1_RGMII	1376.18	Single-ended 50ohm
M1	AB4	ET1_RXD2/CAM_DATA9/SSI0_RCK/MTIOC0D/GTIOC2B/P35_1	ET1_RGMII	1149.03	Single-ended 50ohm
N1	AB3	ET1_RXD3/CAM_DATA10/SSI0_TXD/MTIOC3C/GTETRGA/P36_0	ET1_RGMII	1027.65	Single-ended 50ohm
L1	AG17	DSI_CLKP	MIPI_DSI	541.77	Increment 100ohm
K2	AG18	DSI_CLKN	MIPI_DSI	541.65	
AB10	AH16	DSI_DATA0_P	MIPI_DSI	553.16	Increment 100ohm
AB11	AJ16	DSI_DATA0_N	MIPI_DSI	552.34	
AC8	AH17	DSI_DATA1_P	MIPI_DSI	544.80	Increment 100ohm
AC9	AJ17	DSI_DATA1_N	MIPI_DSI	545.23	
AC5	AH15	DSI_DATA2_P	MIPI_DSI	590.56	Increment 100ohm
AC6	AJ15	DSI_DATA2_N	MIPI_DSI	587.01	
AB4	AH18	DSI_DATA3_P	MIPI_DSI	579.26	Increment 100ohm
AB5	AJ18	DSI_DATA3_N	MIPI_DSI	578.10	
B4	AG13	CSI_CLKP	MIPI_CSI	1691.79	Increment 100ohm
B3	AG12	CSI_CLKN	MIPI_CSI	1688.77	

B1	AJ13	CSI_DATA0_P	MIPI_CSI	1690.87	Increment 100ohm
C1	AH13	CSI_DATA0_N	MIPI_CSI	1694.55	
A3	AJ12	CSI_DATA1_P	MIPI_CSI	1702.11	Increment 100ohm
A2	AH12	CSI_DATA1_N	MIPI_CSI	1702.20	
A6	AJ14	CSI_DATA2_P	MIPI_CSI	1740.83	Increment 100ohm
A5	AH14	CSI_DATA2_N	MIPI_CSI	1742.73	
B7	AJ11	CSI_DATA3_P	MIPI_CSI	1696.86	Increment 100ohm
B6	AH11	CSI_DATA3_N	MIPI_CSI	1697.94	
M4	AJ27	DISP_CLK	Display Out	1972.96	Single-ended 50ohm
K3	AH27	DISP_HSYNC	Display Out	2107.22	Single-ended 50ohm
L3	AJ28	DISP_VSYNC	Display Out	1848.89	Single-ended 50ohm
Y7	AJ19	DISP_DATA0	Display Out	1073.92	Single-ended 50ohm
AA6	AH19	DISP_DATA1	Display Out	950.32	Single-ended 50ohm
Y6	AJ20	DISP_DATA2	Display Out	1057.96	Single-ended 50ohm
AA5	AH20	DISP_DATA3	Display Out	1066.47	Single-ended 50ohm
Y5	AJ21	DISP_DATA4	Display Out	1172.79	Single-ended 50ohm
Y4	AH21	DISP_DATA5	Display Out	1362.73	Single-ended 50ohm
W4	AJ22	DISP_DATA6	Display Out	1379.68	Single-ended 50ohm

V3	AH22	DISP_DATA7	Display Out	1536.66	Single-ended 50ohm
V4	AG22	DISP_DATA8	Display Out	606.34	Single-ended 50ohm
U3	AF22	DISP_DATA9	Display Out	672.06	Single-ended 50ohm
T3	AE22	DISP_DATA10	Display Out	657.94	Single-ended 50ohm
T4	AE23	DISP_DATA11	Display Out	633.75	Single-ended 50ohm
R4	AF23	DISP_DATA12	Display Out	722.98	Single-ended 50ohm
R3	AG23	DISP_DATA13	Display Out	839.84	Single-ended 50ohm
P3	AG26	DISP_DATA14	Display Out	766.02	Single-ended 50ohm
N3	AF27	DISP_DATA15	Display Out	751.43	Single-ended 50ohm
N4	AJ23	DISP_DATA16	Display Out	864.14	Single-ended 50ohm
M3	AH23	DISP_DATA17	Display Out	900.91	Single-ended 50ohm

3 Electrical Characteristics

3.1 Working environment

Environmental parameters	Minimum	Typical	Maximum
Operating temperature	-40°C	/	85°C
Storage temperature	-50°C	/	90°C

Operating humidity	35%（no condensation）	/	75%（no condensation）
Storage humidity	35%（no condensation）	/	75%（no condensation）
Operating voltage	4.5V	5.0V	5.5V
RTC voltage	2.4V	3V	3.6V
RTC current	/	10uA	/

3.2 GPIO DC Characteristics

Parameter name	Mark	Specification				Description
		Minimum	Typical	Maximum	Unit	
High level input voltage	VIH	2	--	3.5	V	--
Low level input voltage	VIL	0	--	0.8	V	--
High level output voltage	VOH	2.4	--	--	V	--
Low level output voltage	VOL	--	--	0.2	V	--

Parameter name	Mark	Specification				Description
		Minimum	Typical	Maximum	Unit	
High level input voltage	VIH	0.7xVDD	--	NVCC_3V3	V	--
Low level input voltage	VIL	0	--	0.2xVDD	V	--
High level output voltage	VOH	VDD - 0.2	--	--	V	--
Low level output voltage	VOL	--	--	0.2	V	--

3.3 Power Consumption Parameters

Operating state	Voltage Typical	Current Typical	Power Consumption Typical
Free state	5.0V	0.24A	1.24W
Fully loaded state	5.0V	0.482A	2.41W

Note: Power consumption is measured based on the evaluation board. The test data is related to specific application scenarios and is for reference only.

Free state: the system starts up, the evaluation board is not connected to other external modules, and the program is not executed.

Fully loaded state: the system is booted, the evaluation board is not connected to other external modules, and the DDR pressure read/write test program is running, the resource utilization of the two ARM Cortex-A53 cores is about 100%.

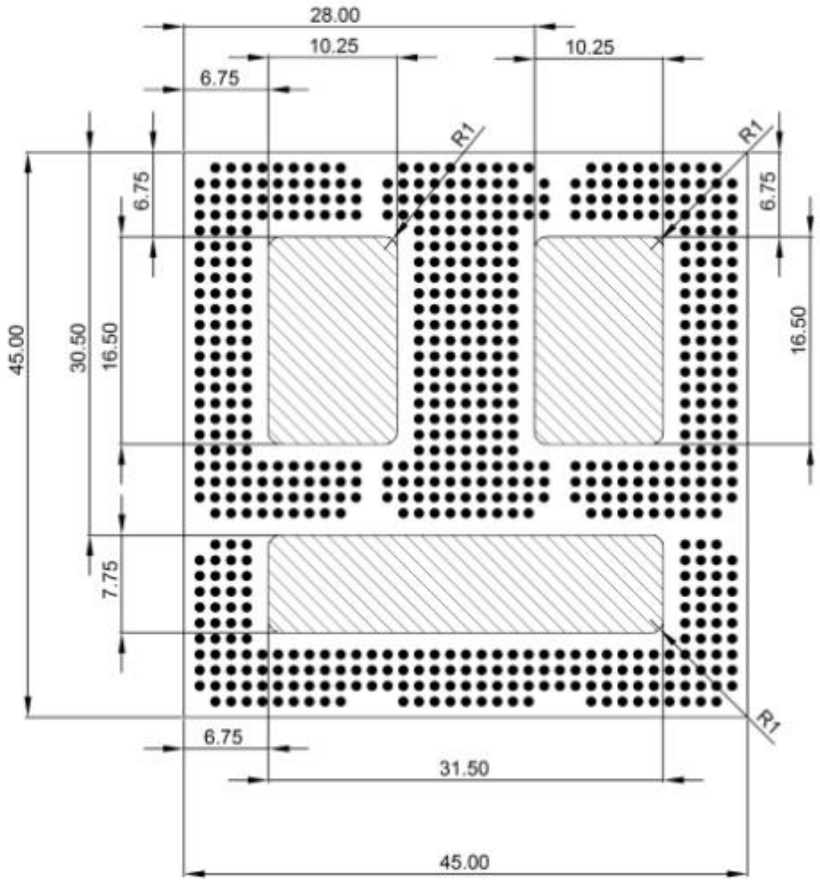
3.4 Core board interface speed

Parameter name	Specification				Description
	Minimum	Typical	Maximum	Unit	
Serial communication rate	--	115200	--	bps	--
SPI communication rate	--	--	52	MHz	--
IIC communication rate	--	100	400	Kbps	--
CAN communication rate	--	--	1	Mbps	--
SD/SDIO communication rate	--	--	104	Mbps	--
USB interface rate	--	--	480	Mbps	--
AD Acquisition time	0.7	--	1.25	uS	Fadc=40 MHz

4 Mechanical Dimensions

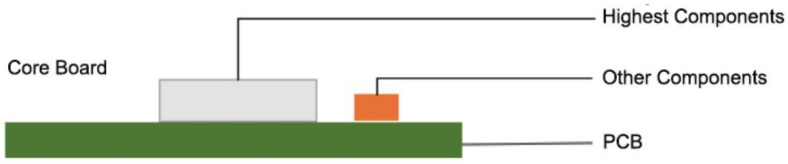
The main hardware-related parameters of the core board are shown below for reference only.

PCB Size	45mm*45mm
PCB Layers	10 layers
PCB Board Thickness	1.2mm
Maximum component height	2.8mm
Weights	15.0g



Core board mechanical dimensions

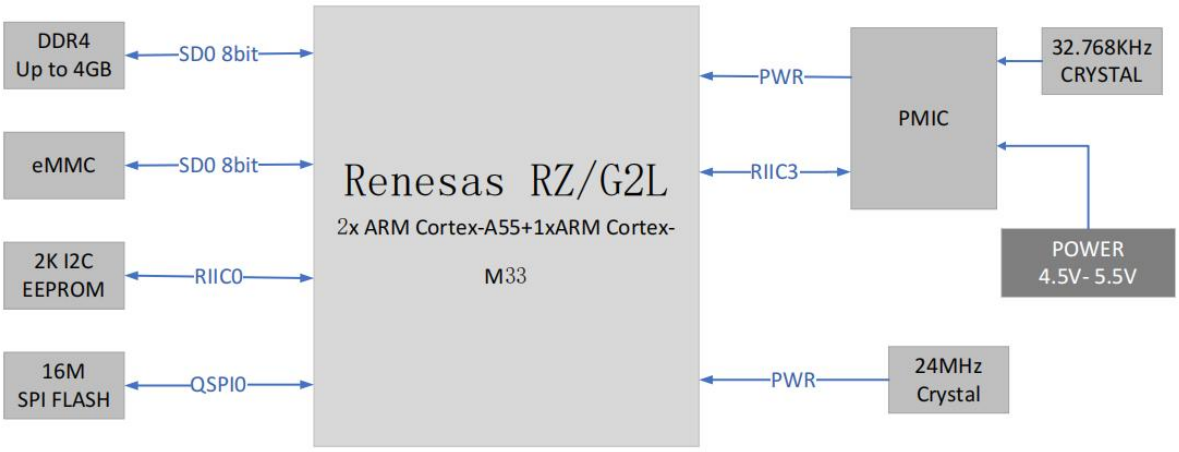
Maximum component height: the height difference between the highest component level of the core board and the level of the PCB front side. The highest component of the core board is the shield cover.



Schematic diagram of the highest devices on the core board

5 G2L Core Board Minimal System Design

G2L core board has integrated the G2L processor, DDR memory, eMMC memory, and PMIC power management circuitry. The system block diagram is shown in Fig.



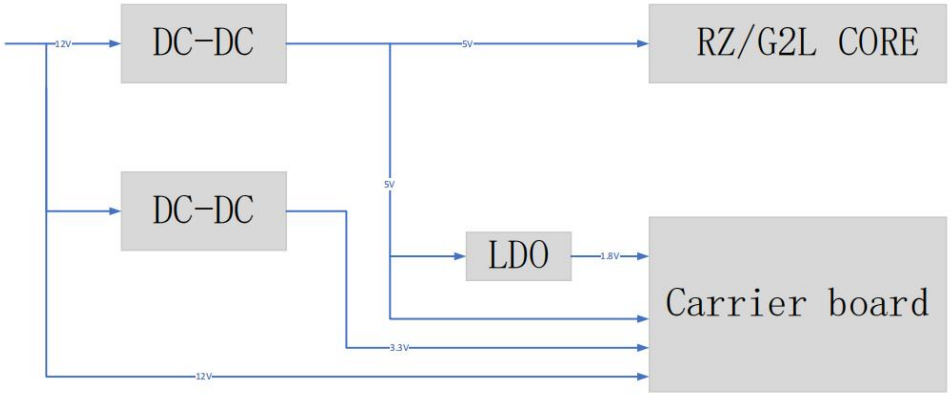
G2L Core Board System Block Diagram

To realize the minimum system, the baseboard needs to complete the following parts of the circuit design.

5.1 Input Power

The core board needs to provide a 5V power supply with a drive current of no less than 2A. It is recommended that a 100uF electrolytic capacitor be added to the 5V input pin to improve power supply stability.

When developing products using the G2L core board, the recommended baseboard power tree is shown in the figure.



Baseboard Power Tree

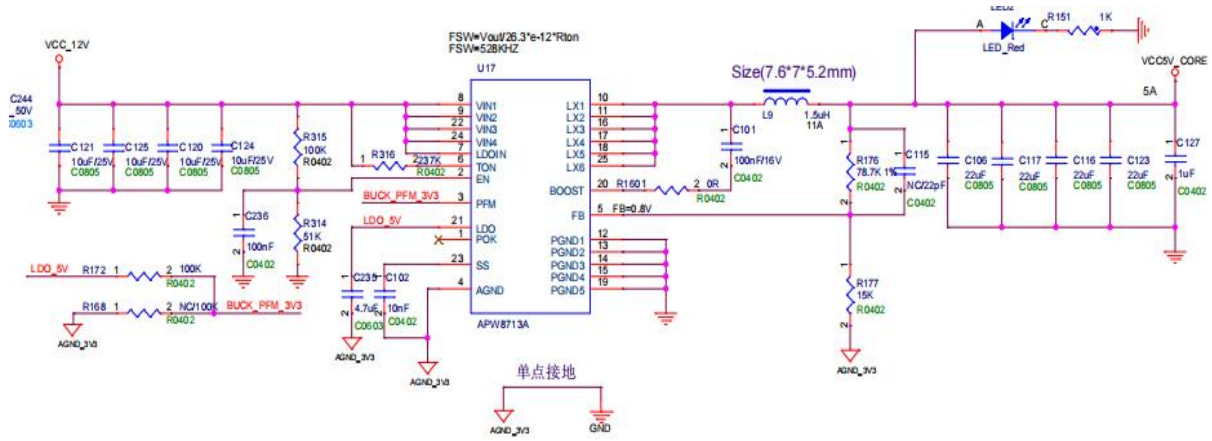
The external power supply VIN is converted to 5V by one DC-DC to supply power to the core board and the base board. The maximum power consumption of the core board is about 2W, and the power consumption of the base board is also taken into account to determine the current to be supplied by the DC-DC.

The other power supplies on the board, such as 3.3V, 1.8V, etc., can be obtained by bucking 5V again. To ensure that the core board is powered up before the chassis, the enable terminals (EN pins) of each DC-DC can be connected to the CARRIER_PWR_ON (V17) output from the G2L core board.

5.2 Recommended Circuits

5.2.1 One-stage conversion circuit

The VIN to 5V recommended circuit is shown in the figure.

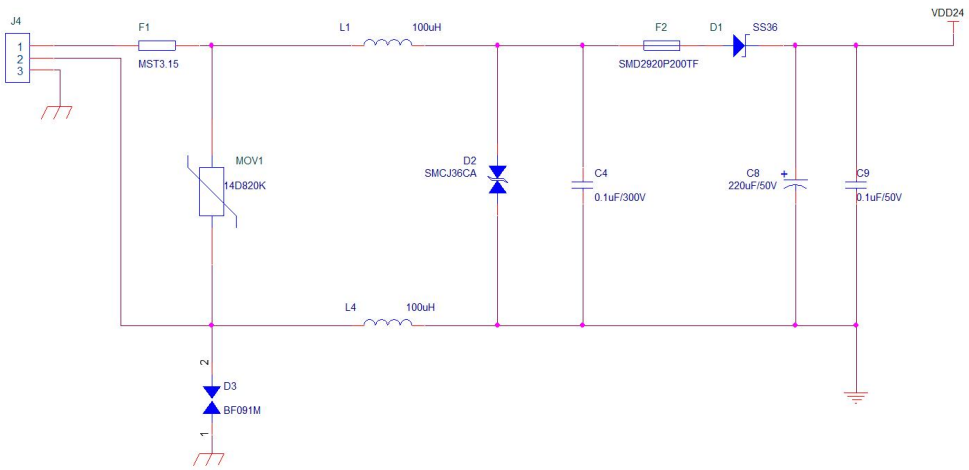


VIN to 5V Recommended Circuit

When the voltage difference between the input and output power supplies is large and the load current is high, the power conversion chip needs to use a DC-DC device with high conversion efficiency, instead of an LDO device, which will burn out the device due to high heat generation.

The reference circuit uses the APW8713A device, which has an input voltage range of 2.7~28V, a maximum output current of 8A, a conversion efficiency of up to 95%, an inductance selectable from 1~4.7uH, and a current rating greater than the load current.

Power Protection Circuit When the environment in which the equipment is located is harsh, such as when it is placed outdoors and may be subjected to lightning strikes, it is necessary to protect the power supply section. The recommended protection circuit is shown in the figure.



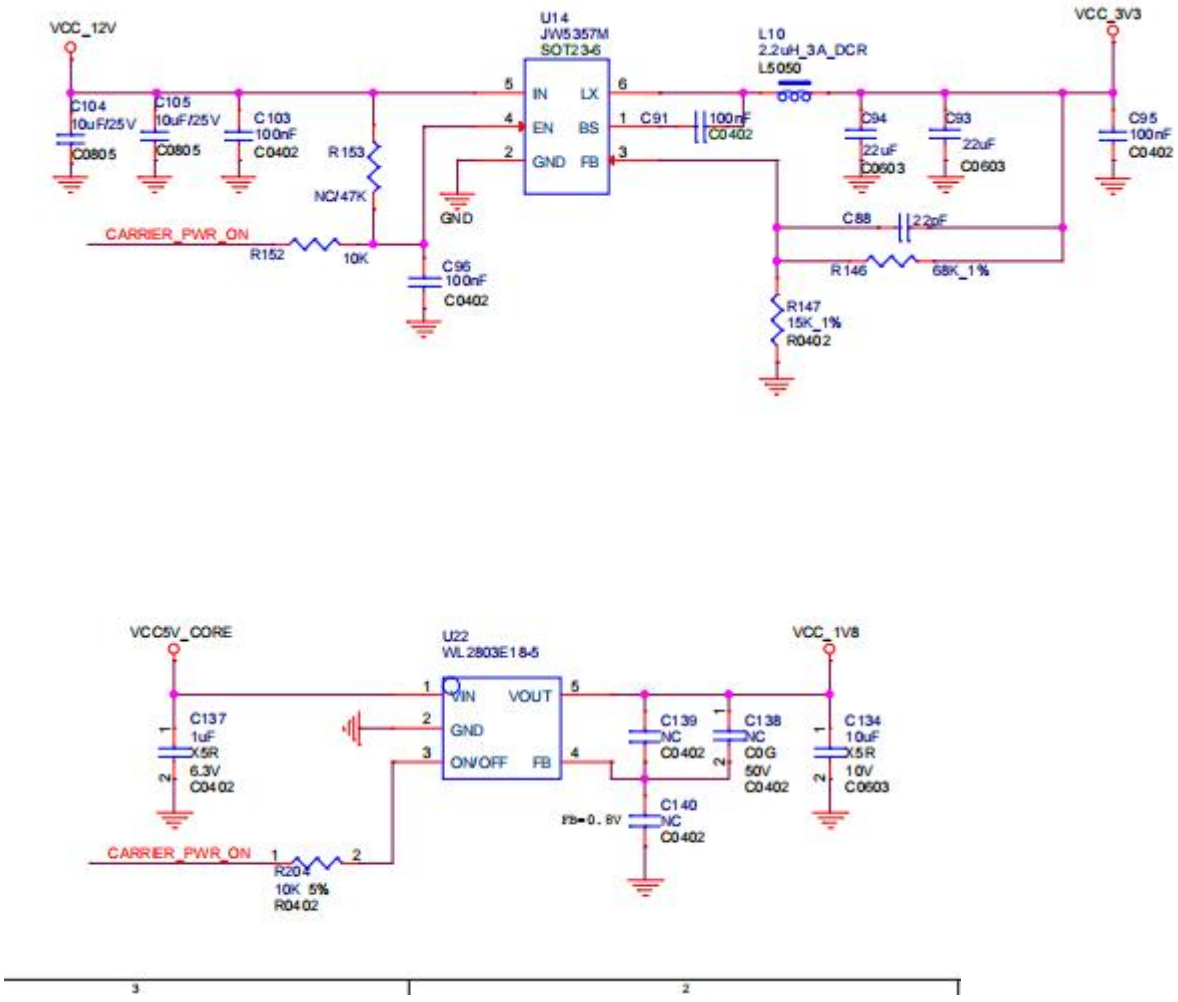
Power Protection Circuit

When surge voltage or current occurs in the power port, varistor MOV1 and gas discharge tube D3 form the first level of protection to absorb the larger surge, and D2 is a TVS tube, which mainly absorbs the residual voltage after the first level of protection. Since the response time of TVS is faster than that of gas discharge tube, in order to prevent TVS from being burnt before the response of gas discharge tube, it is necessary to connect an inductor in series between the two protection circuits to play the effect of time delay.

D1 is a Schottky diode to realize the anti-reverse function.

5.2.2 two-stage conversion circuit

Other power sources on the baseboard, such as 3.3V, 1.8V, etc., can be obtained through 12V\5V step-down again, and the recommended circuit is shown in the figure.



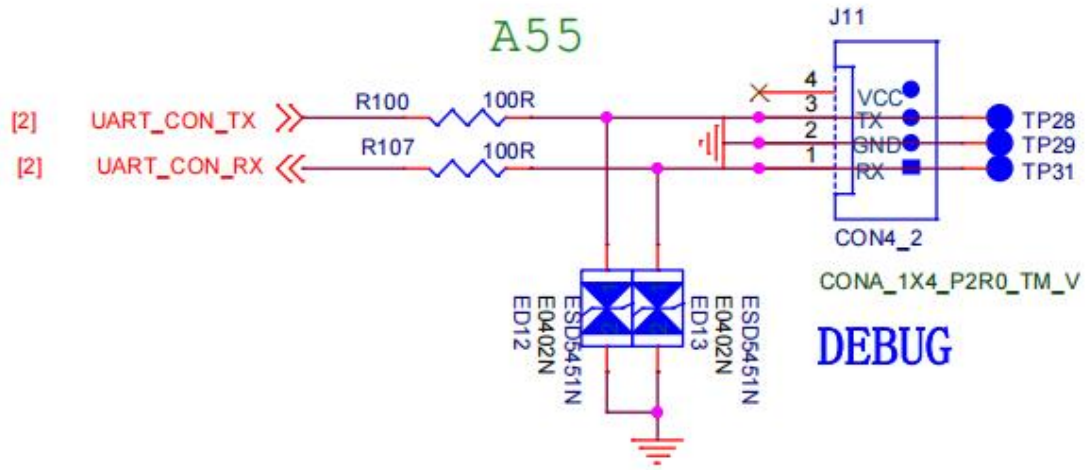
5V to 3.3V Circuit

JW5357M is a two-way power conversion device with a maximum output current of 3A and an adjustable output voltage, and the EN pin is connected to the core board. CARRIER_PWR_ON (V17) on, realizing the timing requirement that the core board is powered up before the base board.

Users can choose other models of power supply devices according to actual needs

5.3 Burn And Debug Interfaces

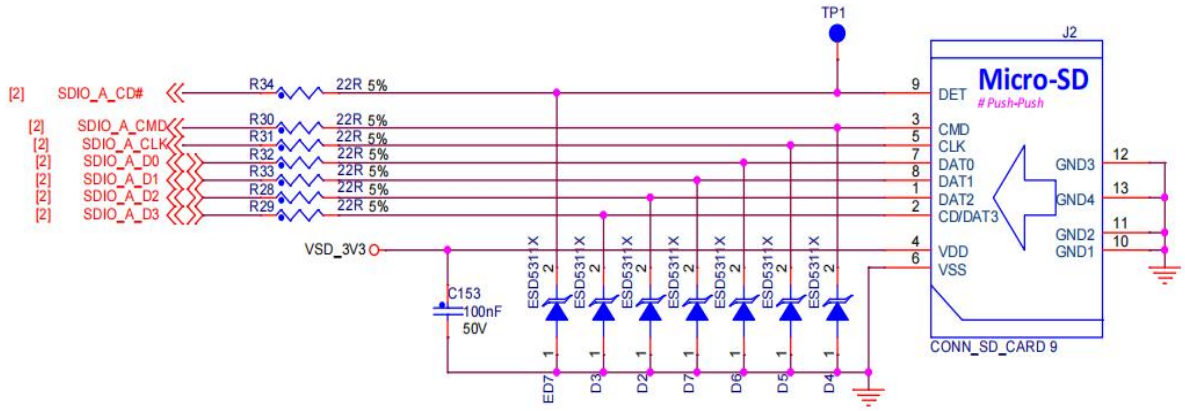
The G2L can only be used for program burning and system debugging through the SCIF0 serial port, so it is necessary to lead out this interface on the backplane, and the interface circuit is shown in the figure.



Burning and debugging serial ports

5.4 TF Card Interface

Veneer in the debugging process, often need to carry out program upgrade operations, therefore, the need to add a TF card interface on the baseboard, the circuit is shown in Figure.



TF Card Interface Circuit

It is recommended to pull up all signals, when PCB wiring, DAT[3:0] and CLK signals need to be processed with equal length, the error is recommended to be 50mil

5.5 BOOT Configuration Interface

G2L processor supports the following boot methods.

MD_BOOT2 to MD_BOOT0			Boot Mode	Interface Module	Connected Device
0	0	0	Boot mode 0	SDHI0	eSD (3.3 V at startup)
0	0	1	Boot mode 1	SDHI0	1.8-V eMMC
0	1	0	Boot mode 2	SDHI0	3.3-V eMMC
0	1	1	Boot mode 3	SPIBSC	1.8-V Single, Quad, or Octal serial flash memory
1	0	0	Boot mode 4	SPIBSC	3.3-V Single or Quad serial flash memory
1	0	1	Boot mode 5	SCIF0	Downloading through SCIF
1	1	0	Reserved	—	Reserved
1	1	1	Reserved	—	Reserved

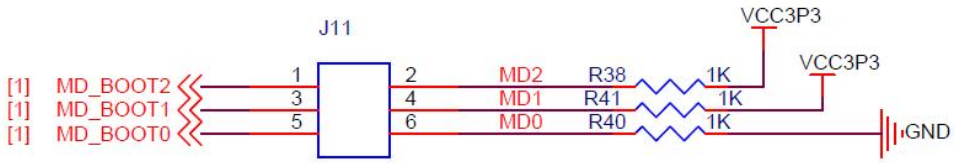
Startup method description:

1) The core board SDHI0 is equipped with an eMMC device and does not support eSD card booting at this time.

2) The default eMMC level on the core board is 1.8V.

3) The core board is equipped with SPI devices and boots from SPI flash by default.

In order to support different boot modes, the BOOT pin needs to be pulled up and down on the backplane, as shown in Figure:



BOOT Pin Configuration Circuit

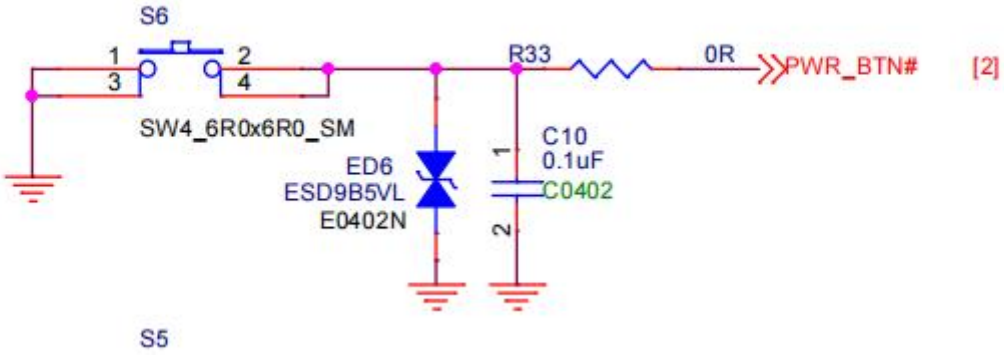
The currently supported startup methods are configured as shown in the following table.

J11 Status	Startup method
0001	SPI FLASH
0100	eMMC
1100	Serial port

Note: 0 indicates that both ends of J11 are disconnected; 1 identifies that both ends of J11 are shorted.

5.6 AA9/PWR_BTN#

AA9/ONOFF is the CPU on/off control pin, press and hold it for more than 5s to turn off the CPU, and press it again for about 1s to switch the CPU on/off.For power on. The core board is designed with a 100K pull-up resistor, please leave it empty when it is not necessary to use.



AA9/ONOFF Pin Circuit Design

6 Manufacturing Welding

1. The workshop life of the modules after unpacking is 24 hours at a temperature of 23 ± 5 °C and a relative humidity of less than 60%. Under these conditions, the modules can be directly reflowed for production or other high-temperature operations. Otherwise, the modules need to be stored in an environment with less than 10% relative humidity (e.g., moisture-proof cabinet) to keep them dry.

2. If the module is in the following conditions, it is necessary to pre-bake the module to prevent the module from absorbing moisture and soldering at high temperatures. PCB blistering, cracking and delamination:

Storage temperature and humidity do not meet recommended storage conditions;

Failure to complete production or storage of the module in accordance with clause 1 above after unpacking;

3. Baking treatment for modules:

Baking at 120 ±5 °C f o r 8 hours is required;

Modules with secondary baking must be soldered within 24 hours of baking, otherwise they must still be stored in the drying oven.

NOTE: The packaging of the modules cannot withstand high temperature baking. Therefore, before baking the module, please remove the module package and place it on a heat-resistant appliance.

4. Production Welding

Use a printing squeegee to print solder paste on the stencil, so that the solder paste will leak through the stencil openings to the PCB, and the strength of the printing squeegee should be adjusted appropriately. In order to ensure the quality of the printed paste on the module, the thickness of the stencil corresponding to the pad portion of the OSMG2L module is recommended to be 0.18~0.20 mm.

The recommended reflow temperature is 238~246 ºC, and the maximum temperature should not exceed 246 ºC. In order to avoid damage to the module due to repeated heat exposure, it is strongly recommended that customers reflow the first side of the PCB board before applying the module. The recommended oven temperature profile (leadfree SMT reflow) and related parameters are as follows

Reflow Temperature Profile

7 Statements

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