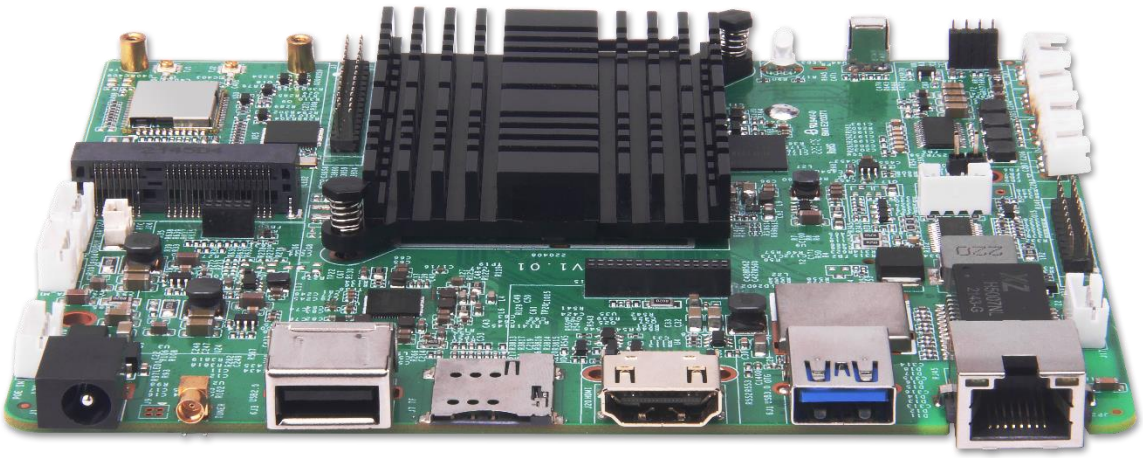
K3-3568

Hardware UserGuide



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Geniatech

Contents

1 Introduction

K3-3568 is an Android Customized Board with following new features:

(I) Quad core ARM Cortex-A55 CPU up to @ 2.0GHz

(II) ARM Mali-G52 GPU, Support OpenGL ES1.1/2.0/3.2, OpenCL2.0 and Vulkan 1.1

(III) NPU: Neural network acceleration engine with processing performance up to 1.0 TOPS

(IV) Support Android 11.0 / Linux Debian

(V) Support 2GB/4GB/8GB LPDDR4, 8~128GB eMMc, External expansion TF/SATA3.0/USB storage

(VI) Peripheral interface：USB2.0 * 1, USB3.0 * 1, RJ45 * 1, Mini RF * 1, SIM Card Slot * 1, DC IN * 1

(VII) Display interface：HDMI OUT * 1, LVDS * 1, eDP * 1，MIPI DSI * 1，HDMI IN * 1(Optional)

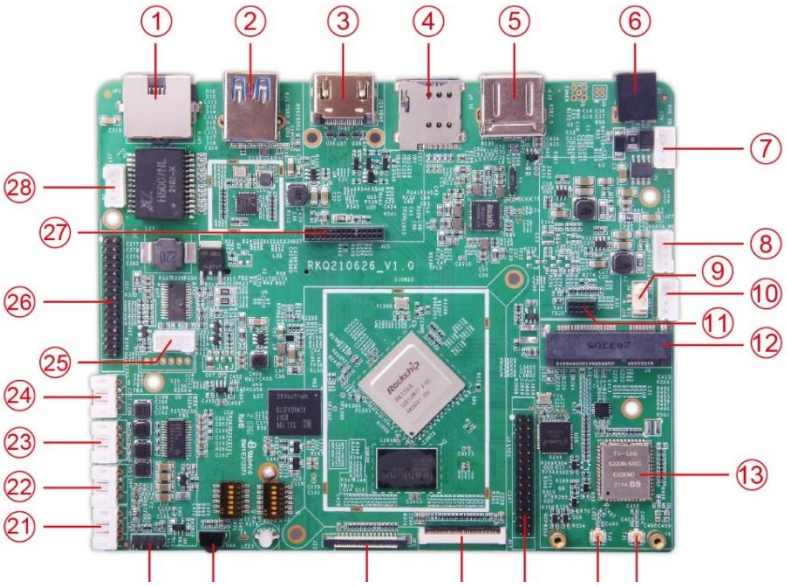
(VIII) Build-in：MIPI CSI * 1, MIPI DSI * 1, Mini PCIe * 1, USB2.0 * 4, Speaker * 1, PDM * 1, I2C * 1, UART * 1

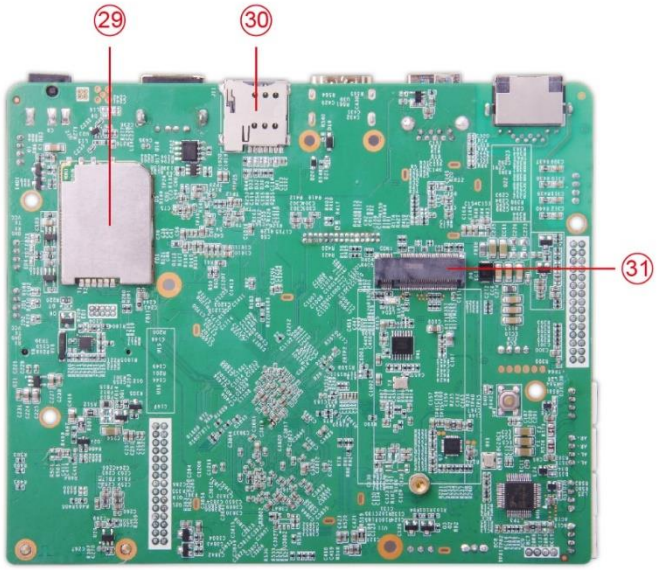
(IX) Network： WIFI5(2.4G+5.8G), BT4.0, GIGA Ethernet * 1 Support hardware WDT & RTC + 1*Speaker (Max: 2*5W8Ω)

(X) Support wide voltage 12V power input, standard EMC and ESD protection design

(XI) Specially designed for smart express cabinet, smart commercial display, smart vending machine, digital signage, smart home, etc.

1.1 Board Overview

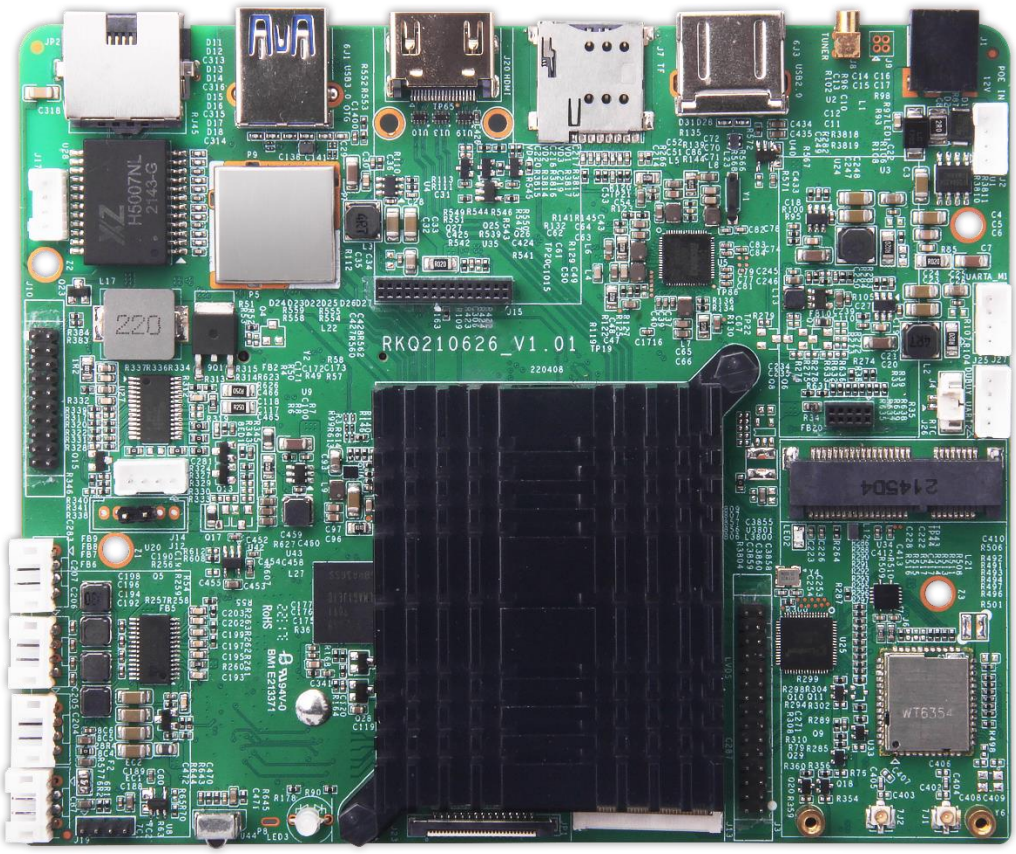


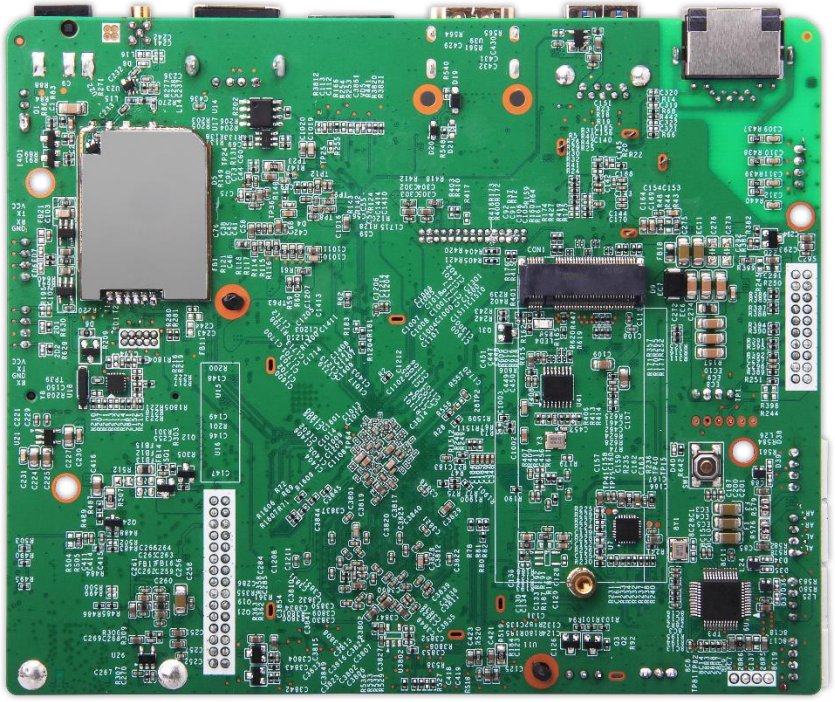


No.	Name	Description
1	RJ45	*1(10/100/1000M Ethernet)
2	USB3.0	*1
3	HDMI Slot	*1（Support HDMI 2.0a）
4	TF Card Slot	*1（Up to 512GB）
5	USB2.0	*1
6	DC IN	*1(12V Adapter)
7	POE In	*1
8	UART	*1
9	RTC Battery In	*1
10	DEBUG	*1
11	GTIoT	*1(External IoT module)
12	MiniPCIe Slot	*1(for 3G/4G module)
13	Wifi Module	*1
14	Wifi Antenna	*2
15		
16	LVDS Slot	*1
17	MIPI DSI Slot	*1
18	MIC Array Slot	*1
19	IR	*1
20	USB Slot	*1(for wifi module)
21	USB Slot	*1
22	USB Slot	*1
23	Speaker Slot	*1
24	USB Slot	*1
25	Backlight Slot	*1
26	eDP Slot	*1
27	HDMI IN Slot	*1
28	POE Out Slot	*1
29	Tuner Module	*1
30	SIM Card Slot	*1
31	M.2 Slot	*1 (for 5G module)

2 What's in the Developer Board

The Developer Board contains one K3-3568.





3 Getting started

3.1 Prerequisites

Before you power up your K3-3568 for the first time you will need the following:

- K3-3568 board
- A K3-3568 board compliant power supply (sold separately by Geniatech).
- A K3-3568 board compliant IR remote (sold separately by Geniatech).
- A LVDS or eDP LCD Monitor that supports a resolution of Max to 2560x1600@60Hz.
- LVDS-LVDS cable or eDP-eDP cable to connect the board to the LCD.
- A computer keyboard/mouse with USB interface.

3.2 Starting the board for the first time

To start the board, follow these simple steps:

step 1. Connect the LVDS / eDP cable to the DS3566 connector (marked) and to the LCD Monitor.

step 2. Connect the keyboard to the boards USB connector marked or connect the mouse to the USB connector marked. (It doesn't matter which order you connect it in. You can also connect via an external USB Hub.)

step 3. Connect the power supply to power connector marked.

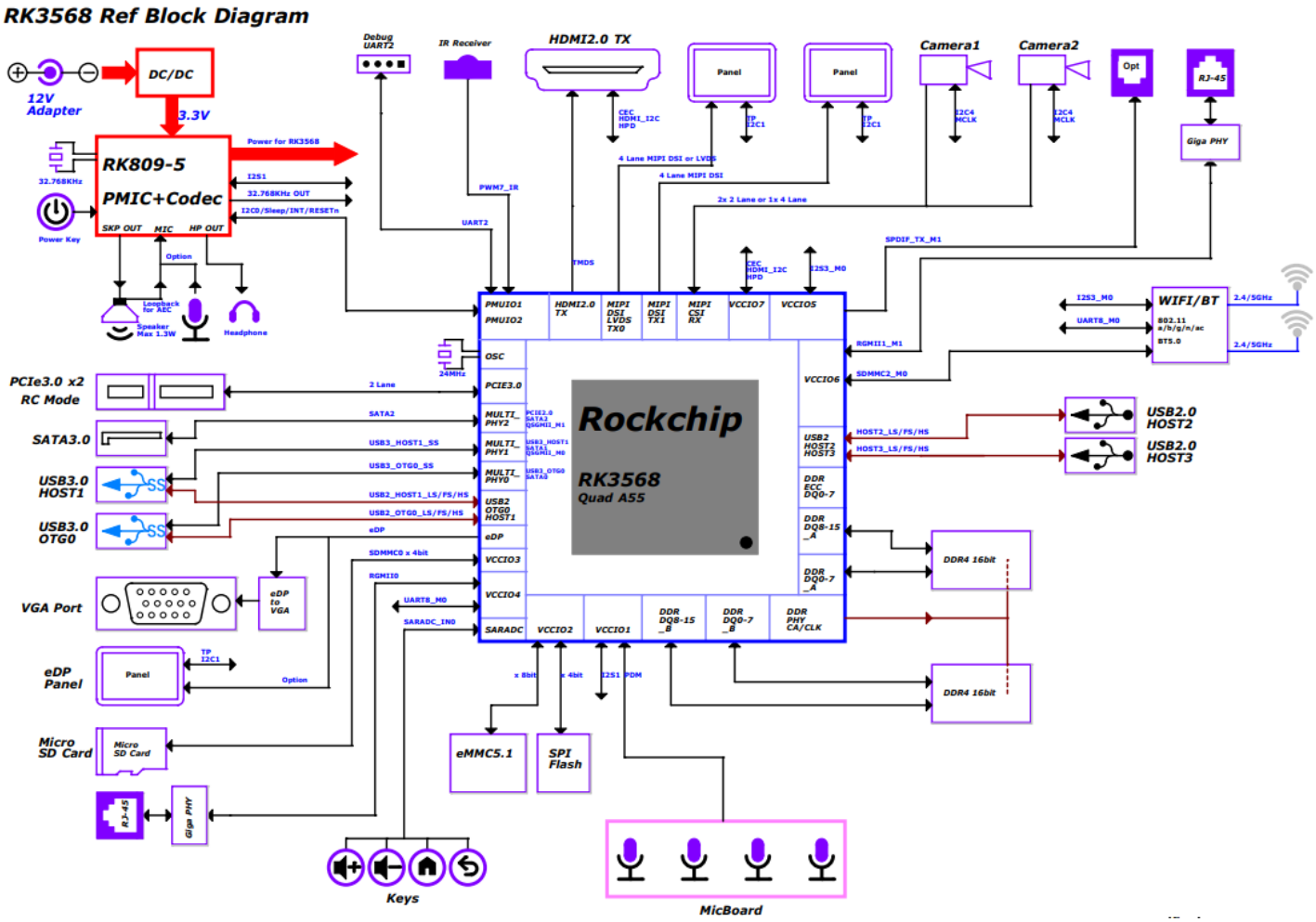
Power on (Plug power adapter), toggle the power switch, then the board will boot up and you will see the boot up logo with Android.

Please note that the first boot takes several minutes due to Androids initialization. Subsequent boot times should be faster.

4. K3-3568 Overview

4.1 Product Diagram

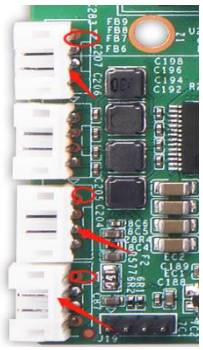
Block Diagram:



4.2 Internal Connectors, Headers & Jumpers

USB Slot (J21/J22/J24)

No.	Function	Property	Description
1	VCC	POWER	Output 5V
2	DM	Input/Output	USB2.0 data -
3	DP	Input/Output	USB2.0 data +
4	GND	Ground	



Debug(J25)

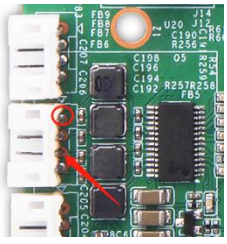
No.	Function	Property	Description
1	VCC	POWER	Output 5V or 3.3V
2	TX	Output	UART TX
3	GND	Ground	
4	RX	Input	UART RX

UART (J27)

No.	Function	Property	Description
1	VCC	POWER	Output 5V or 3.3V
2	TX	Output	TX
3	GND	Ground	
4	RX	Input	RX

SPEAKER(J23)

No.	Function	Property	Description
1	AL+	Output	Audio left channel+
2	AL-	Output	Audio left channel-
3	AR-	Output	Audio right channel-
4	AR+	Output	Audio right channel+

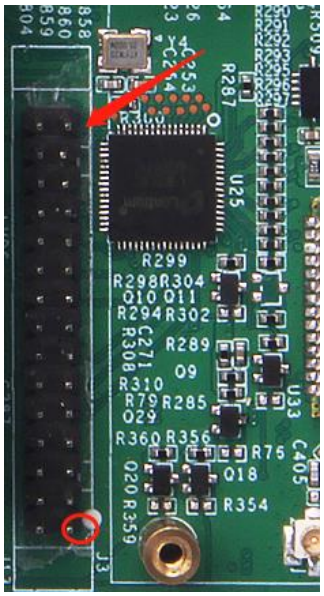


BACKLIGHT(J18/J19)

No.	Function	Property	Description
1	VCC	Power	Output 12V
2	VCC	Power	Output 12V
3	EN	Output	Back light Control ON/OFF
4	ADJ	Output	Back light adjust brightness
5	GND	Ground	
6	GND	Ground	

LVDS(J3)

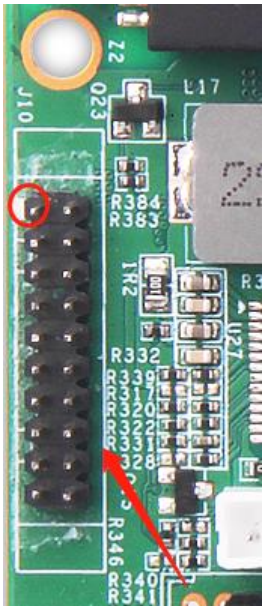
No.	Function	Property	Description
1	VDD	POWER	Output 12V/5V/3.3V
2	VDD		
3	VDD		
4	GND	Ground	
5	GND		
6	GND		
7	LVDS0_DN0	Output	Channel 0 D0 data signal
8	LVDS0_DP0	Output	
9	LVDS0_DN1	Output	Channel 0 D1 data signal
10	LVDS0_DP1	Output	
11	LVDS0_DN2	Output	Channel 0 D2 data signal
12	LVDS0_DP2	Output	
13	GND	Ground	
14	GND	Ground	
15	LVDS0_CLKN	Output	Channel 0 Clock data signal
16	LVDS0_CLKP	Output	
17	LVDS0_DN3	Output	Channel 0 D3 data signal
18	LVDS0_DP3	Output	
19	LVDS1_DN0	Output	Channel 1 D0 data signal
20	LVDS1_DP0	Output	
21	LVDS1_DN1	Output	Channel 1 D1 data signal
22	LVDS1_DP1	Output	
23	LVDS1_DN2	Output	Channel 1 D2 data signal
24	LVDS1_DP2	Output	
25	GND	Ground	
26	GND	Ground	
27	LVDS1_CLKN	Output	Channel 1 Clock data signal
28	LVDS1_CLKP	Output	



29	LVDS1_DN3	Output	Channel 1 D3 data signal
30	LVDS1_DP3	Output	

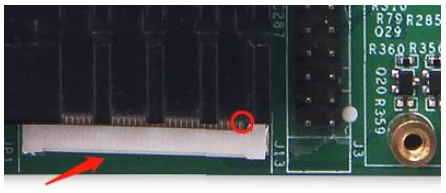
eDP(J17)

No.	Function	Property	Description
1	VDD	POWER	Output 12V/5V/3.3V
2	VDD		
3	GND	Ground	
4	GND		
5	D0-	Output	Lane0 data signal
6	D0+	Output	
7	D1-	Output	Lane1 data signal
8	D1+	Output	
9	D2-	Output	Lane2 data signal
10	D2+	Output	
11	D3-	Output	Lane3 data signal
12	D3+	Output	
13	GND	Ground	
14	GND	Ground	
15	AUX-	Output	AUX Channel signal
16	AUX+	Output	
17	GND	Ground	
18	GND	Ground	
19	HPD	Output	Hotplug
20	VCC	POWER	Output 3.3V



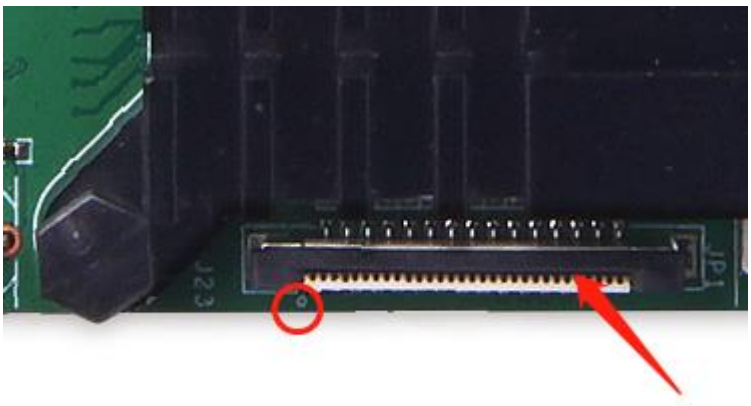
MIPI DSI(J10)

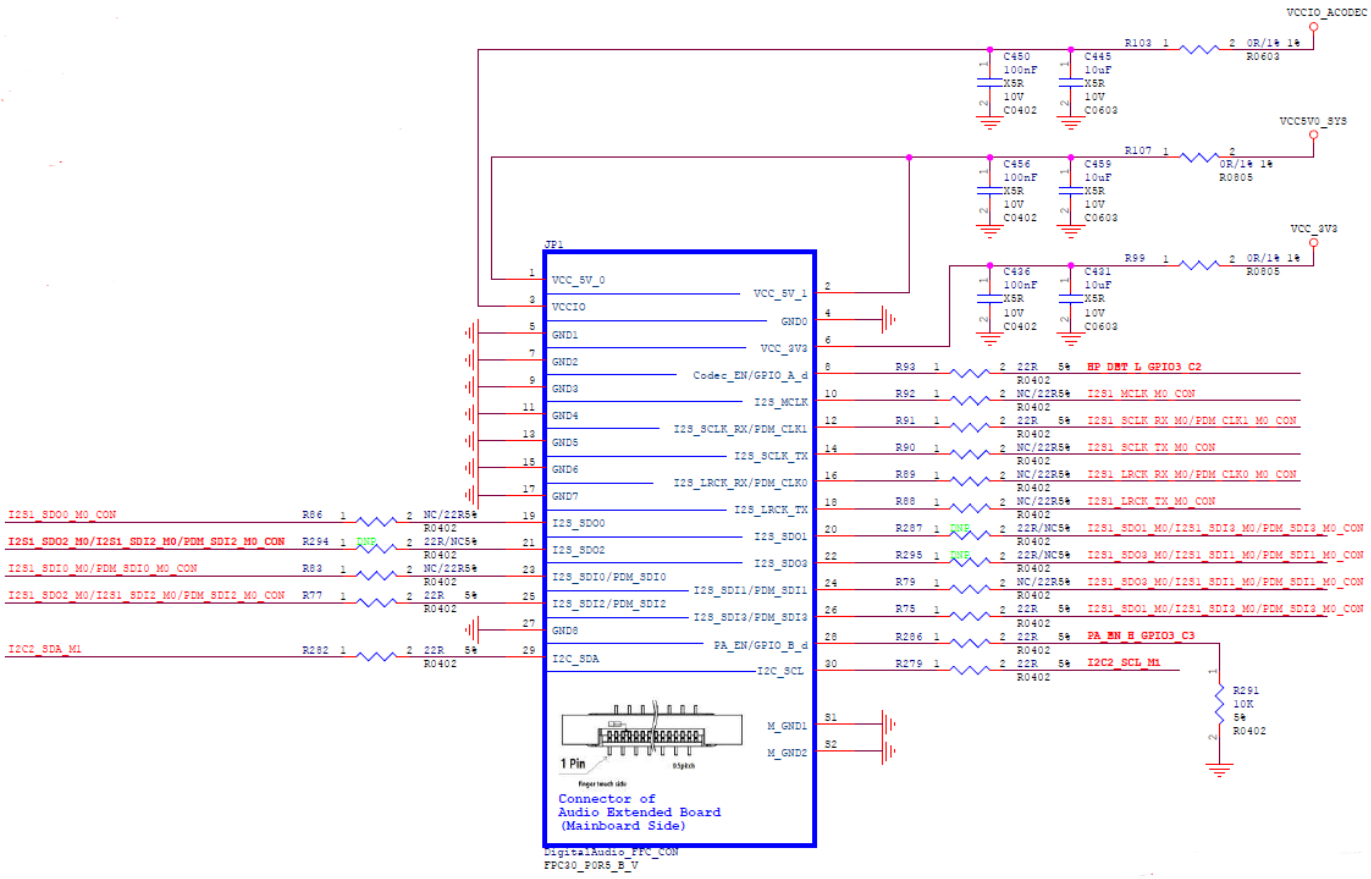
No.	Function	Property	Description
1	VCC	POWER	Output 3.3V
2	VCC	POWER	
3	NC		
4	EN	Output	BackLight Control ON/OFF
5	PWR	POWER	BackLight Control Brightness
6	SDA	Input/Output	I2C Data signal
7	SCL	Input/Output	I2C Clock signal
8	NC		
9	GND	Ground	
10	DP2	Output	MIPI Lane 2 Signal



11	DN2	Output	
12	GND	Ground	
13	DP1	Output	MIPI Lane 1 Signal
14	DN1	Output	
15	GND	Ground	
16	CLKP	Output	MIPI Clock Signal
17	CLKN	Output	
18	GND	Ground	
19	DP0	Output	MIPI Lane 0 Signal
20	DN0	Output	
21	GND	Ground	
22	DP3	Output	MIPI Lane 3 Signal
23	DN3	Output	
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	GND	Ground	Reset
28	ID	Output	
29	NC/GND		
30	NC		
31	VDD	POWER	Output 5V
32	VDD		
33	VDD		
34	VDD		

PDM(JP1)




VCCIO_ACODEC
VCC5V0_SYS
VCC_3V3
JP1
VCC_5V_0
VCCIO
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
I2C_SDA
VCC_5V_1
GND0
VCC_3V3
Codec_EN/GPIO_A_d
I2S_MCLK
I2S_SCLK_RX/PDM_CLK1
I2S_SCLK_TX
I2S_LRCK_RX/PDM_CLK0
I2S_LRCK_TX
I2S_SDO0
I2S_SDO1
I2S_SDO3
I2S_SDI0/PDM_SDI0
I2S_SDI1/PDM_SDI1
I2S_SDI2/PDM_SDI2
I2S_SDI3/PDM_SDI3
PA_EN/GPIO_B_d
I2C_SCL
M_GND1
M_GND2
1 Pin
Connector of
Audio Extended Board
(Mainboard Side)
DigitalAudio_FFC_CON
FFC30_F0R5_B_V
HP_DET_L_GPIO3_C2
PA_EN_H_GPIO3_C3
I2C2_SCL_M1
I2S1_SDO0_M0_CON
I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0_CON
I2S1_SDI0_M0/PDM_SDI0_M0_CON
I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0_CON
I2C2_SDA_M1
I2S1_MCLK_M0_CON
I2S1_SCLK_RX_M0/PDM_CLK1_M0_CON
I2S1_SCLK_TX_M0_CON
I2S1_LRCK_RX_M0/PDM_CLK0_M0_CON
I2S1_LRCK_TX_M0_CON
I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0_CON
I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0_CON
I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0_CON
I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0_CON

4.3 System Block Diagram