# DB-G2L-V2 Industrial Development Board hardware manual

## Revision History

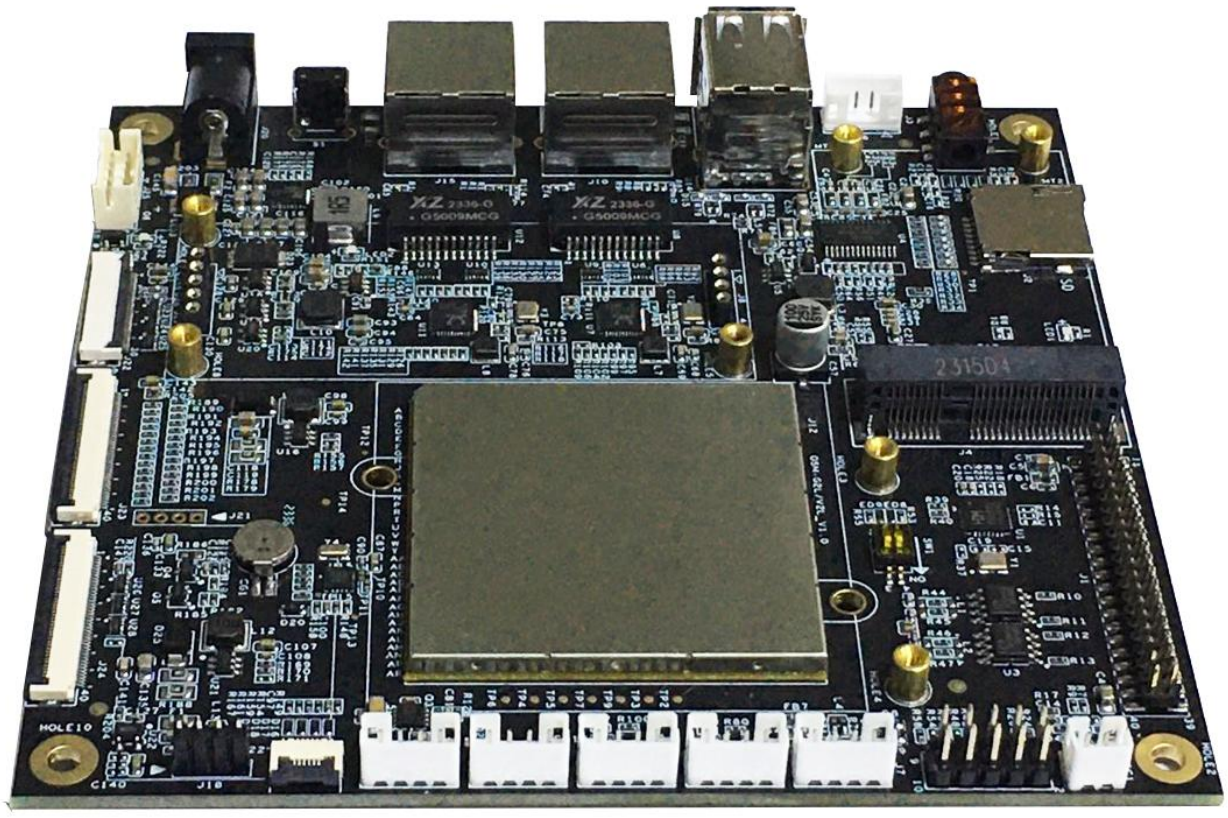
| Draft Date | Revision No. | Description |
|---|---|---|
| 2023/10/12 | V1.0 | Initial version. |

# CONTENTS

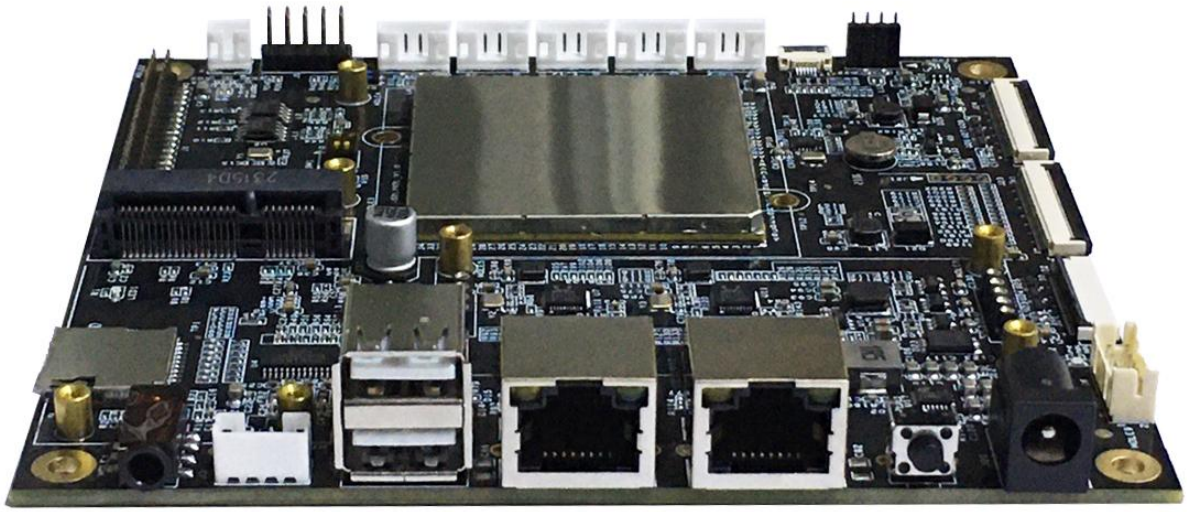
## 1 Hardware Introduction

DB-G2L-V2 is a high-performance industrial development board based on the industrial-grade Renesas RZ/G2L dual-core ARM Cortex-A55 + single-core ARM Cortex-M33 heterogeneous multicore processor design, consisting of a core board and a backplane. the ARM Cortex-A55 main processing unit clocked at 1.2GHz, integrates the latest high-performance ARM Cortex-A55 main processing unit with 1.2GHz, integrated with the latest high-performance CPU and GPU, and also adopts a security island with Cortex-R5 dual-core lock-step mode, which can be applied to scenarios with stringent requirements on security performance.

The development board is rich in interface resources, leading to a dual-channel network port, 2x CAN-bus, 3x USB2.0, multiple serial ports, on-board USB WiFi module, support for 4G module, while leading to MIPI LCD, CAMERA, RGB LCD, LINE IN, LINE OUT, MIC IN and other audio and video multimedia interfaces, so that the user can quickly carry out the evaluation of product solutions and technology pre-research. and technology pre-study.



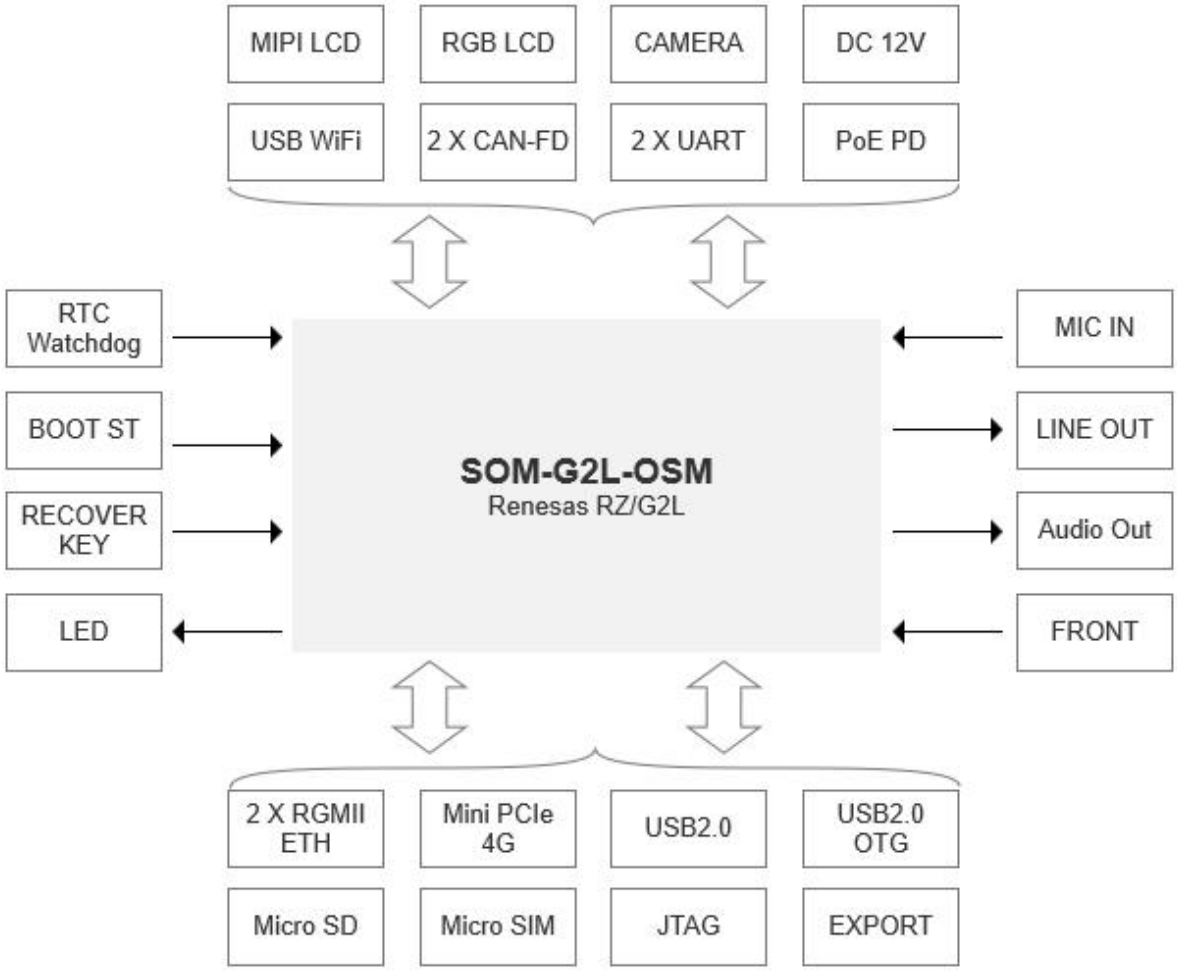
Development board front view



Development board side view

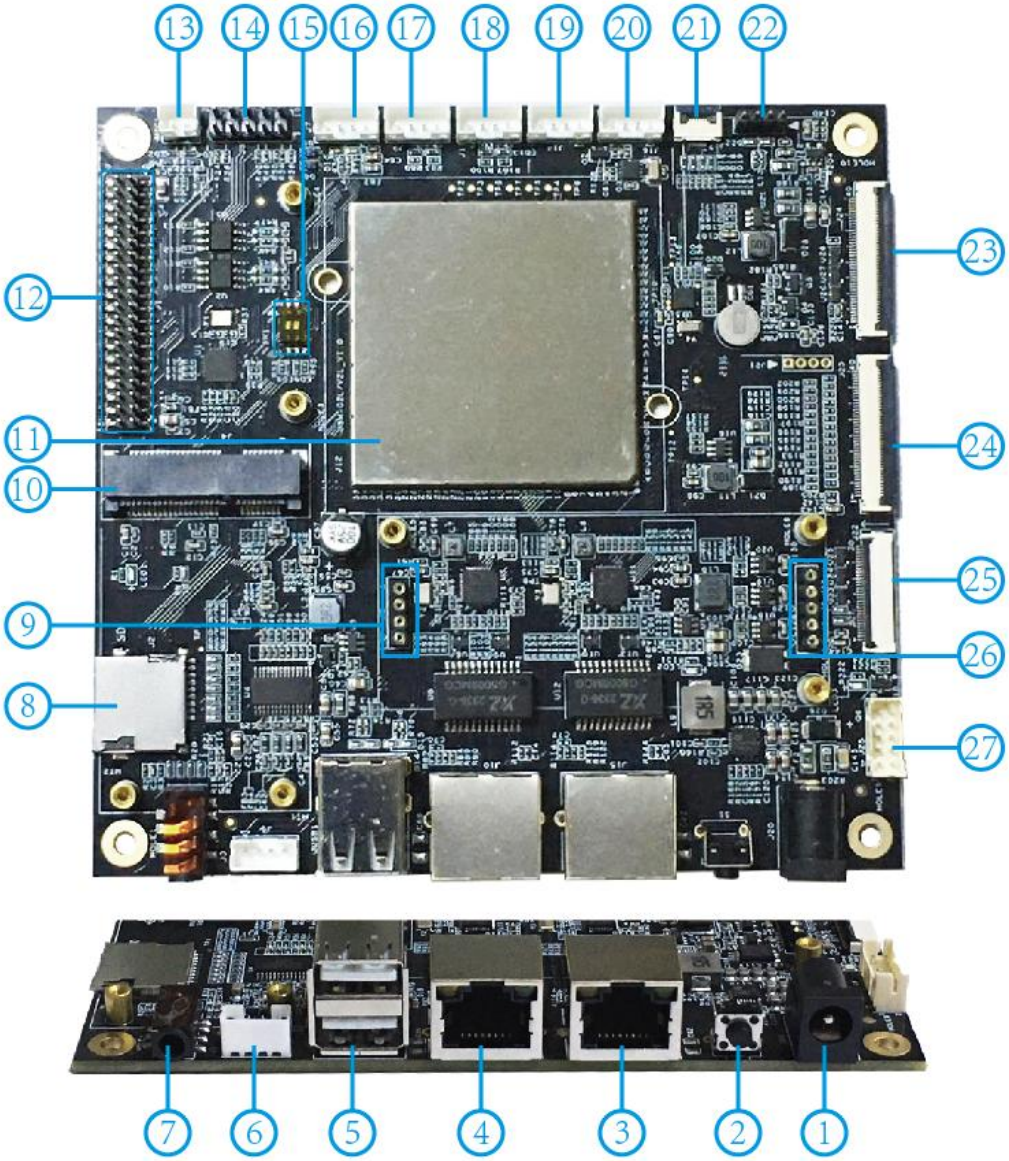
# 2 Software And Hardware Parameters

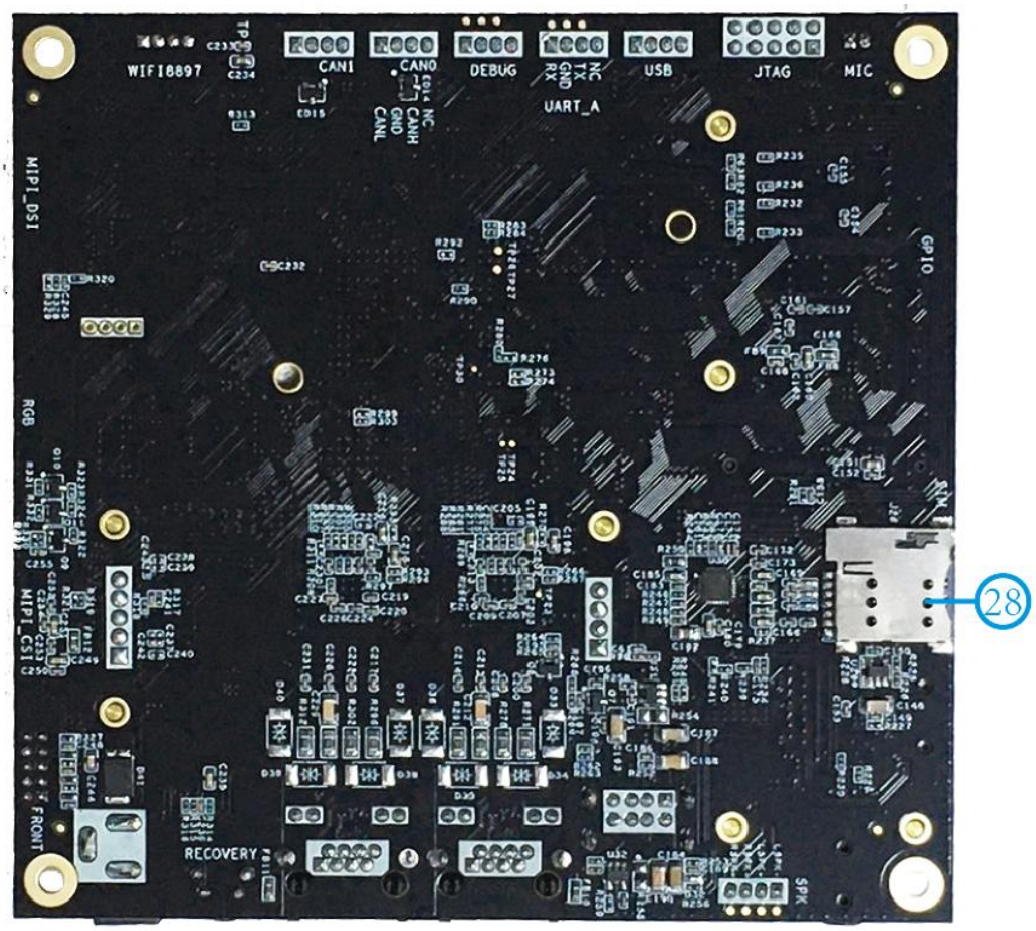
## 2.1 Hardware Block Diagram




Development board hardware block diagram

## 2.2 Development Board Interface Definitions






Development board interface definition diagram

| No. | Label | Functional Description | Remark |
|---|---|---|---|
| 1 | J20 | DC Power Interface | 1x 12V input power connector for 5.5mm OD, 2.1mm ID power plugs |
| 2 | S1 | RECOVER Key | Access to the system burn-in button |
| 3 | J15 | Ethernet-2 | RJ45 ethernet-2 interface |
| 4 | J10 | Ethernet-1 | RJ45 ethernet-1 interface (PoE PD support, optional) |
| 5 | JUSB1 | USB2.0 | 1x USB2.0 HOST(USB2 HUB) Type A lower level<br>1x USB2.0 OTG Type A upper level<br>Remarks:After the USB_B bus i s expanded with four signals through the USB2.0 HUB, one of the signals is led out directly.<br>USB_A bus direct lead |
| 6 | J6 | SPK | 1x 4PinWhite Terminal Block, 2.0mm Spacing |
| 7 | J3 | Audio | 1x LINE OUT+MIC IN connector, 3.5mm audio cradle |
| 8 | J2 | Micro SD | 1x Micro SD card slot |

| | | | |
|---|---|---|---|
| 9 | J8 | PoE PD Input | 1x 4Pin Black Row Holder, 2.0mm Spacing |
| 10 | J4 | 4G | 1x Mini PCIe connected via USB2.0 HUB |
| 11 | J13 | SOM-G2L-OSM Core boards | 1x 662Pin LGA |
| 12 | J1 | EXPORT | 1x EXPORT Expansion Connector, 2x20pin Pin Header, 2.0mm Pitch |
| 13 | MIC1 | MIC | 1x 2Pin white terminal block, 2.0mm spacing |
| 14 | J5 | JTAG | 2x 5Pin header，2.54mm spacing |
| 15 | SW1 | BOOT SET | 1x 2bit boot mode selection dip switch |
| 16 | J7 | USB2.0 touch screen interface | 1x 4Pin white terminal block, 2.0mm spacing |
| 17 | J9 | UART | 1x 4Pin white terminal block, 2.0mm spacing |
| 18 | J11 | Debut | 1x 4Pin white terminal block, 2.0mm spacing |
| 19 | J14 | CAN-FD-1 | 1x 4Pin white terminal block, 2.0mm spacing |
| 20 | J16 | CAN-FD-2 | 1x 4Pin white terminal block, 2.0mm spacing |
| 21 | J17 | Capacitive Touch Screen Interface | 1x 6Pin FFC connector, 0.5mm spacing |
| 22 | J18 | USB WiFi | 1x 4Pin Pin Array, 2.0mm Spacing Connects via USB2.0 HOST |
| 23 | J24 | MIPI LCD interface | 1x 40Pin FFC Connector, 0.5mm Spacing |
| 24 | J23 | RGB LCD interface | 1x 40Pin FFC Connector, 0.5mm Spacing |
| 25 | J22 | CAMERA | 1x 30Pin FFC Connector, 0.5mm Spacing |
| 26 | J19 | PoE PD Output | 1x 5Pin Black Row Holder, 2.0mm Spacing |
| 27 | J25 | FRONT | 2x5pin header, 2.0mm spacing |
| 28 | J26 | Micro SIM | 1x 4G Micro SIM card slot |

## 2.3 Hardware Parameters

| | |
|---|---|
| CPU | Renesas RZ/G2L |
| | 2x ARM Cortex-A55，1.2GHz main frequency, support floating point function |
| | ARM Cortex-M33,dedicated real-time processing unit at 200MHz |
| | VPU：Encoding / Decoding support H.264 / AVC (High Profile / Main Profile / Baseline Profile)，H.264 / MVC (Stereo High Profile)，maximum pixel rate: 1920 x 1080 x 30 fps |
| | GPU：Mali-G31 500MHz，support OpenGL ES 1.1/2.0/3.1/3.2、Vulkan 1.1、OpenCL 2.0 |

| | |
|---|---|
| | ISU： Maximum input image resolution: 5M (2800×2047)， Maximum output image resolution: Full HD (1920×1080)，support color format conversion: RGB / ARGB / YcbCr422 / YcbCr420 / RAW(Grayscale) |
| ROM | 16/32GB eMMC<br>128Mb SPI FLASH |
| RAM | 2GB DDR4 |

## 2.4 Peripheral Configuration

The main peripheral configurations and performance parameters are shown in the following table.

| Peripheral Interface | Quantities | **Performance Parameters** |
|---|---|---|
| MIPI CSI | 1 | 1x CAMERA， 30pin FFC connector, 0.5mm spacing |
| MIPI DSI | 1 | 1x MIPI LCD, 40pin（display）FCC connector + 6pin（capacitive touch screen）FFC connector, 0.5mm spacing, Maximum resolution support up to 1920 x 1080@60fps |
| DVP | 1 | 1x 40Pin FFC connector with 0.5mm spacing, supports WXGA（1280 × 800）60fps |
| USB HOST | 1 | USB 2.0 Type A（supports up to 480 Mbps） |
| USB OTG | 1 | USB 2.0 Type A（supports up to 480 Mbps） |
| WiFi | 1 | USB WiFi, 4pin Black Terminal Block, 2.0mm Pitch<br>Note: After the USB_B bus expands four signals through the USB2.0 HUB, one of the expansion signals The signal is then expanded through the USB2.0 HUB. |
| Ethernet | 2 | 2x RJ45 interfaces, RMII/RGMII support, 10/100/1000Mbps network adaptive;<br>The first Ethernet supports PoE PD. |
| 4G | 1 | Mini PCIe interface via USB2.0 HUB |
| Micro SD | 1 | Micro SD card slot |
| CAN FD | 2 | 2x 4 pin white terminal blocks, 2.0mm spacing |
| SPK | 1 | 4 pin white terminal blocks, 2.0mm spacing |
| LINE OUT+MIC IN | 1 | 3.5mm Audio holder |
| MIC | 1 | 2 pin white terminal blocks, 2.0mm spacing |
| JTAG | 1 | Supports JTAG debugging interface |
| RTC | 1 | Suitable for button cell MS621 (3V rechargeable) |

| | | | | |
|---|---|---|---|---|
| Watchdog | 1 | 1x Watchdog | | |
| Debug | 1 | Debug UART white terminal blocks, 2.0mm spacing | | |
| UART | 1 | UART 4 pin white terminal blocks, 2.0mm spacing | | |
| I2C | 1 | 6pin FFC connector with 0.5mm pitch | | |
| BOOT SET | 1 | 2bit startup mode selection dip switch | | |
| POWER | 1 | 12V DC input power connector for 5.5mm OD, 2.1mm ID power plugs | | |
| EXPORT | 1 | SPI | 2 | 2x 20Pin black pins, 2.0mm spacing |
| | | UART | 4 | |
| | | I2C | 1 | |
| | | GPIO | 5 | |
| | | 5V | 1 | |
| | | 3.3V | 1 | |

## 2.5 Software Parameters

| | | |
|---|---|---|
| Kernel | 4.19 | |
| Uboot | 2020.10 | |
| OS | Yocto | |
| Driver support | eMMC | DDR4 |
| | MMC/SD | LED |
| | KEY | USB WIFI/4G/Mouse |
| | UART | I2C |
| | CAN-FD | MIPI CAMERA |
| | MIPI LCD | Ethernet |
| | LINE IN/OUT | Touch Screen |
| | RTC | |

### 2.6 Development Information

- Provide core board pin definition, core board 3D graphic files, editable base board schematic, editable base board PCB, chip Data sheet, shorten the hardware design cycle.
- Provides file system images, kernel driver source code, and a wealth of demo programs
- Provides complete platform development kits, getting started tutorials to save time on software organization and make application development easier.

## 3 Electrical Characteristics

### 3.1 Operating Environment

| Environmental Parameters | Minimum | Typical | Maximum |
|---|---|---|---|
| Operating temperature | -40°C | / | 85°C |
| Storage temperature | -50°C | / | 90°C |
| Operating humidity | 35%（no condensation） | / | 75%（no condensation） |
| Storage humidity | 35%（no condensation） | / | 75%（no condensation） |
| Operating voltage | 9V | 12.0V | 18V |

### 3.2 GPIO DC Characterization

| Parameters | Label | Specifications | | | | Remark |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | Unit | |
| High level input voltage | VIH | 2 | -- | 3.5 | V | -- |
| Low level input voltage | VIL | 0 | -- | 0.8 | V | -- |
| High level output voltage | VOH | 2.4 | -- | -- | V | -- |
| Low level output voltage | VOL | -- | -- | 0.2 | V | -- |

| Parameters | Label | Specifications | | | | Remark |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | Unit | |

| | | | | | | |
|---|---|---|---|---|---|---|
| High level input voltage | VIH | 0.7xVDD | -- | NVCC_3V3 | V | -- |
| Low level input voltage | VIL | 0 | -- | 0.2xVDD | V | -- |
| High level output voltage | VOH | VDD - 0.2 | -- | -- | V | -- |
| Low level output voltage | VOL | -- | -- | 0.2 | V | -- |

### 3.3 Power Consumption Parameters

| Operating State | Voltage Typical | Current Typical | Power Consumption Typical |
|---|---|---|---|
| Free state | 12.0V | 0.15A | 1.8W |
| Full load state | 12.0V | 0.23A | 2.76W |

Note: Test data is related to specific application scenarios and is for reference only.

Free state: the system is started, the development board is not connected to other external modules, and the program is not executed.

Full load state: the system boots up, the development board is not connected to other external modules, running the DDR pressure read/write test program, the resource utilization of the two ARM Cortex-A53 cores is about 100%.

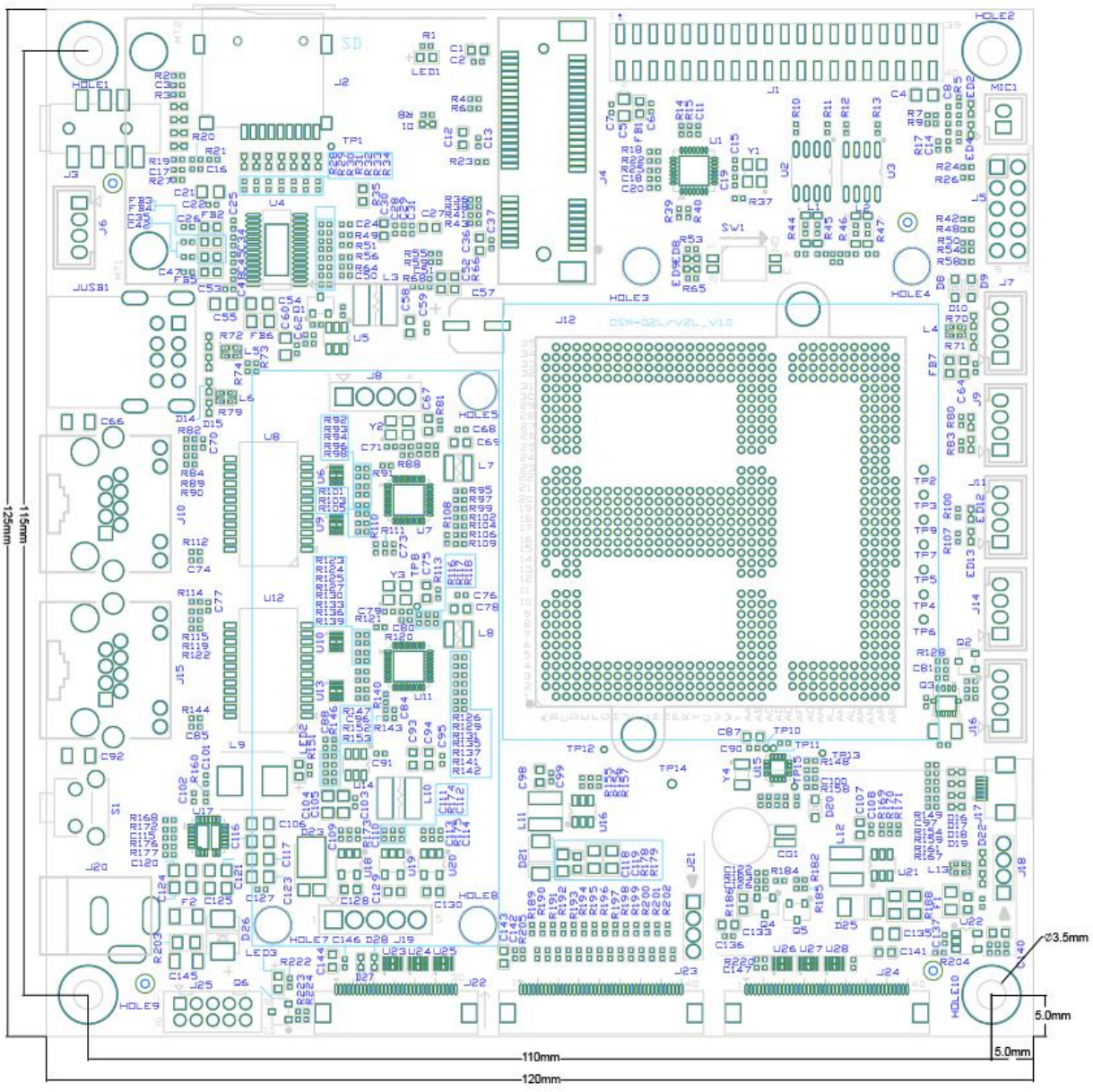
### 3.4 Interface Speed

| Parameters | Specifications | | | | Remark |
|---|---|---|---|---|---|
| | Minimum | Typical | Maximum | Unit | |
| Serial communication speed | -- | 115200 | -- | bps | -- |
| SPI communication speed | -- | -- | 52 | MHz | -- |
| IIC communication speed | -- | 100 | 400 | Kbps | -- |
| CAN communication speed | -- | -- | 1 | Mbps | -- |
| SD/MMC/SDIO | -- | -- | 104 | Mbps | -- |
| USB interface speed | -- | -- | 480 | Mbps | -- |
| AD acquisition time | 0.7 | -- | 1.25 | uS | Fadc=40 MHz |

# 4 Mechanical Dimensions

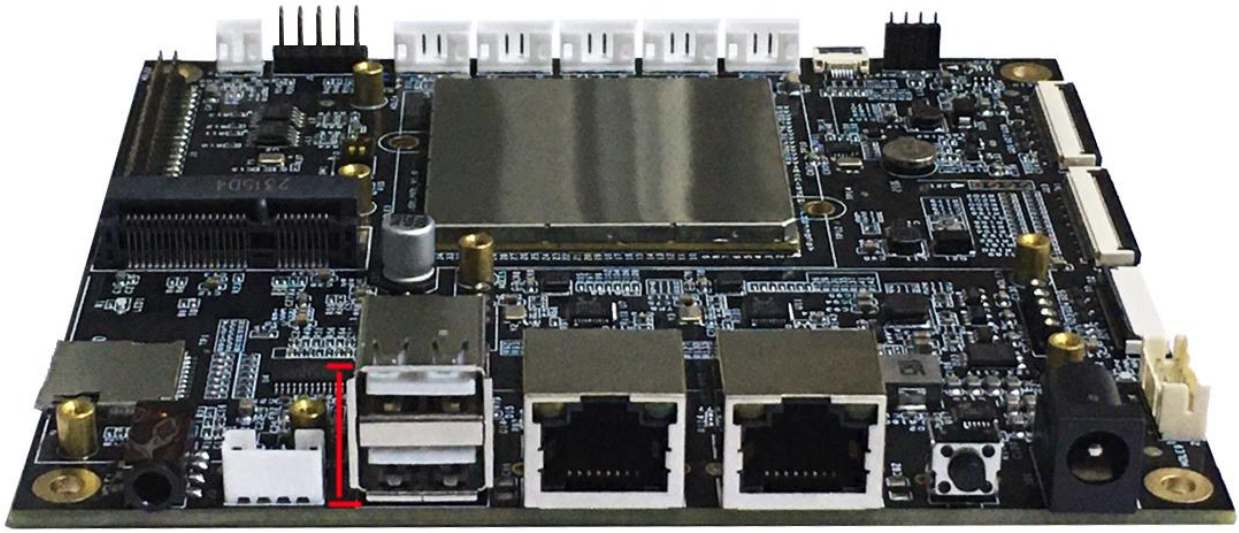
The main hardware-related dimensions of the development board are shown below for reference only.

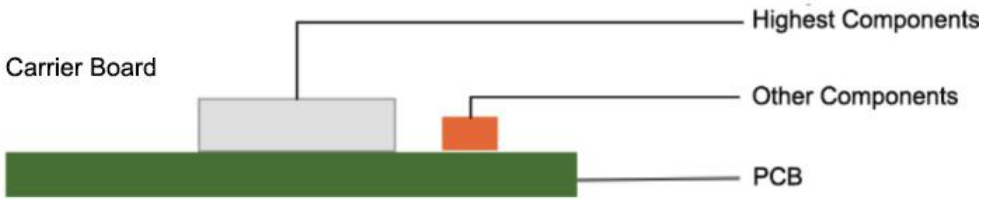
| | |
|---|---|
| PCB Size | 120mm*125mm |
| PCB Layers | 4 Layers |
| PCB Board Thickness | 1.6mm |
| Number of mounting holes | 4 |
| Maximum component height | 22mm |
| Weights | 130g |




Development board mechanical dimensions

Maximum component height: the height difference between the highest component level of the development board and the level of the front of the PCB. The highest component on the board is the duallayer USB sockets(JUSB1).






Schematic of the highest device on the development board

## 5 Development Board Kit List

### 5.1 Standard accessories

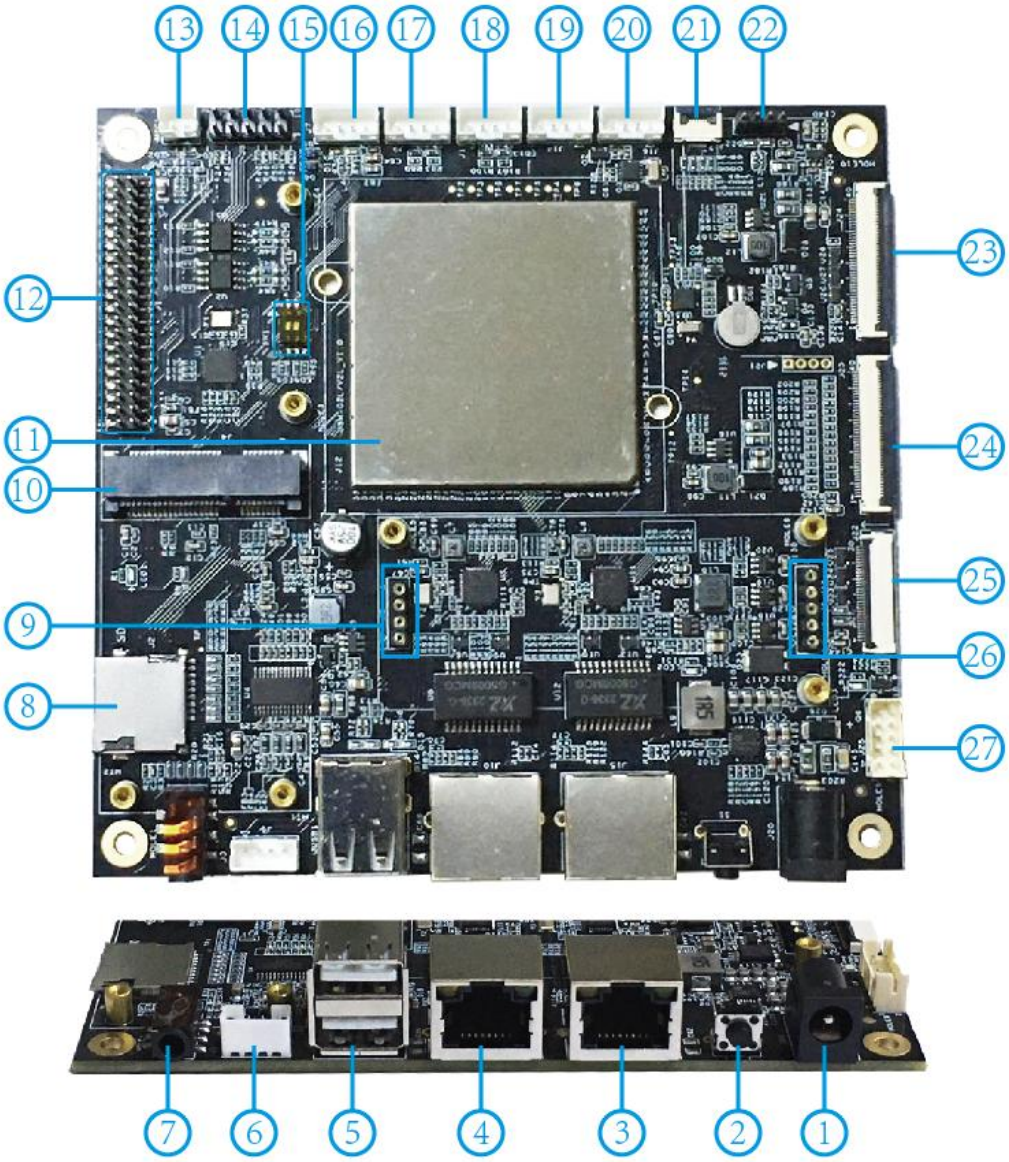
| Name | Quantity | Remark |
|---|---|---|
| Development Board with Core Board | 1 | |
| 12V Power Adapter | 1 | Standard configuration |
| 2.4G Antenna | 1 | Standard when WiFi function is available |

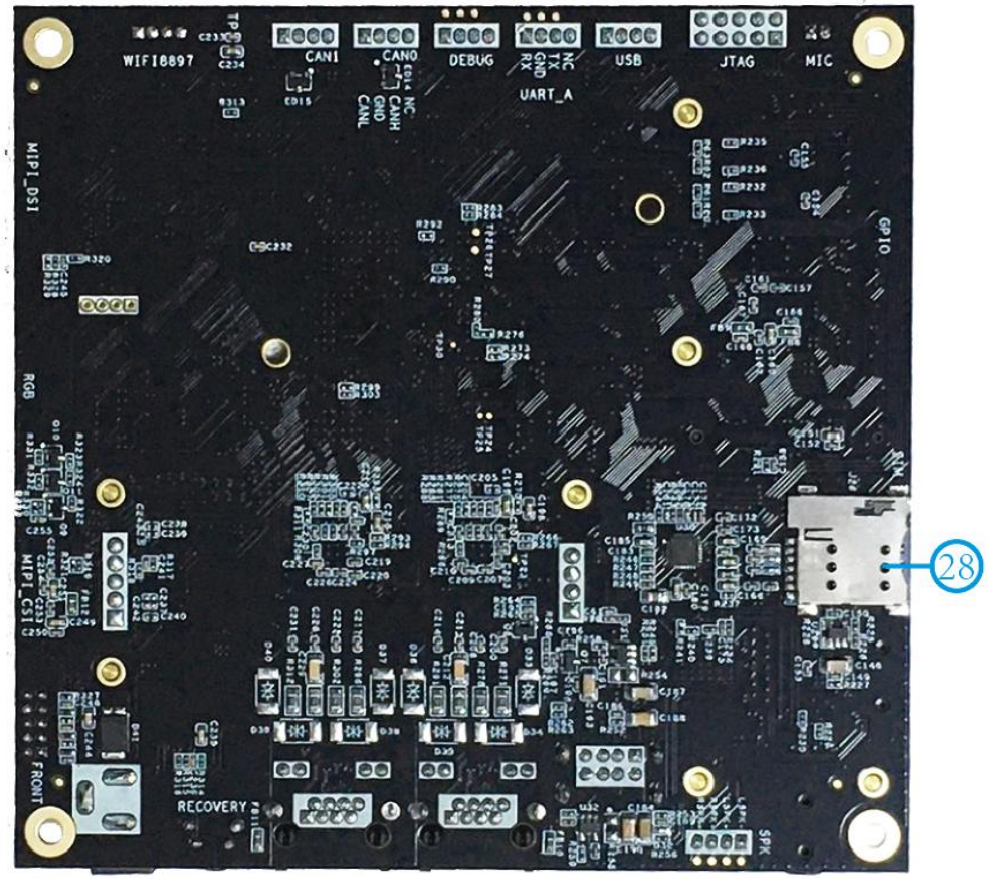
### 5.2 Optional Accessories

| Name | Model | Quantity | Remark |
|---|---|---|---|
| Serial Debugging Tools | | 1 | |

| | | | |
|---|---|---|---|
| 10.1" MIPI LCD with Capacitive Touch | WD101HKM40AB-E6-05/HK101TLEDM-KM01 | 1 | 1280x800 |
| 7" MIPI LCD with Capacitive Touch | AML070JGI50-07403L-A | 1 | 1024x600 |
| 4.3" RGB LCD with Capacitive Touch | AVD-TT43WQ-CW-234-A SP | 1 | 480x272 |
| 4.3" RGB LCD with Capacitive Touch | HX043JGI50-43103 | 1 | 800x480 |
| PoE PD Module | POE-12V | 1 | |
| MIPI CSI Camera | ZH13850-ZH-001 | 1 | |
| 4G Module | EC25 | 1 | Mini PCIe interface |
| WiFi Module | 88W8897 | 1 | USB2.0 interface |

## 6 Development Board Interface Definitions

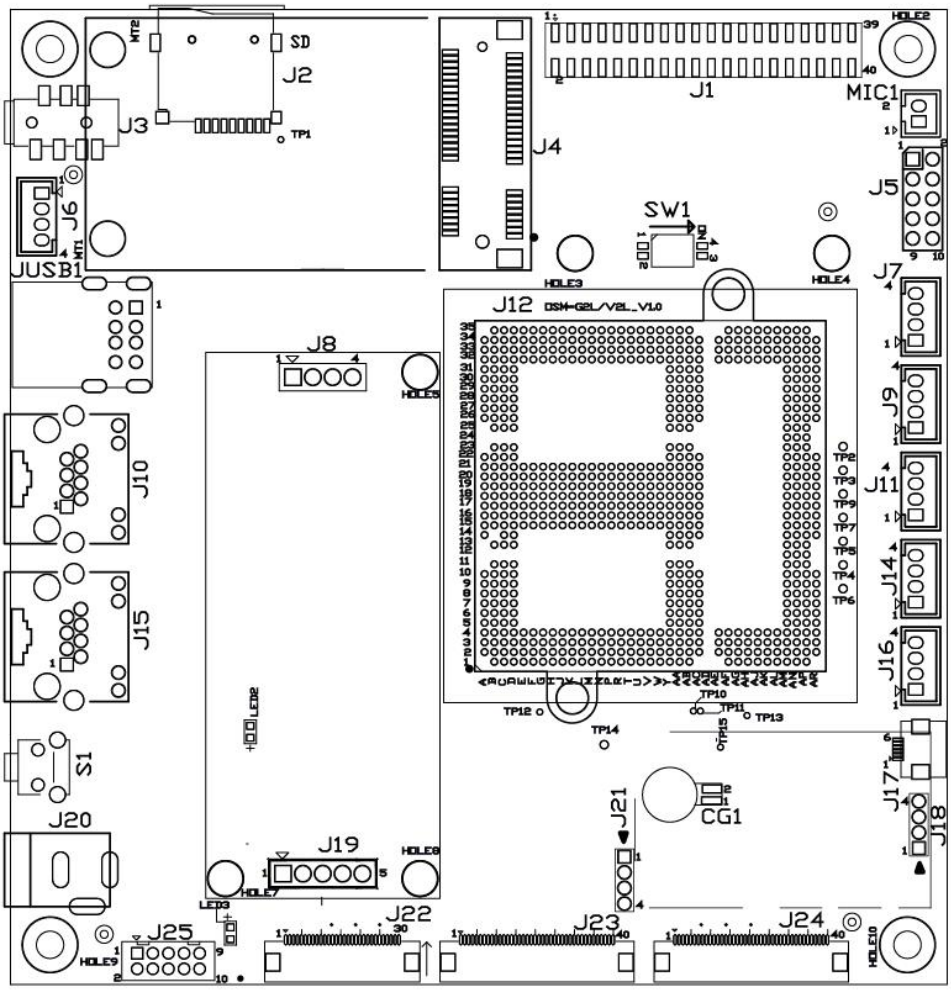





Development Board interface definition diagram

| No. | Label | Functional Description | Remark |
|---|---|---|---|
| 1 | J20 | DC Power Interface | 1x 12V input power connector for 5.5mm OD, 2.1mm ID power plugs |
| 2 | S1 | RECOVER Key | Access to the system burn-in button |
| 3 | J15 | Ethernet-2 | RJ45 ethernet-2 interface |
| 4 | J10 | Ethernet-1 | RJ45 ethernet-1 interface (PoE PD support, optional) |
| 5 | JUSB1 | USB2.0 | 1x USB2.0 HOST(USB2 HUB) Type A lower level<br>1x USB2.0 OTG Type A upper level<br>Remarks:After the USB_B bus i s expanded with four signals through the USB2.0 HUB, one of the signals is led out directly.<br>USB_A bus direct lead |
| 6 | J6 | SPK | 1x 4PinWhite Terminal Block, 2.0mm Spacing |
| 7 | J3 | Audio | 1x LINE OUT+MIC IN connector, 3.5mm audio cradle |
| 8 | J2 | Micro SD | 1x Micro SD card slot |

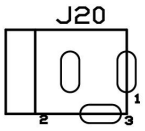
| | | | |
|---|---|---|---|
| 9 | J8 | PoE PD Input | 1x 4Pin Black Row Holder, 2.0mm Spacing |
| 10 | J4 | 4G | 1x Mini PCIe connected via USB2.0 HUB |
| 11 | J13 | SOM-G2L-OSM Core boards | 1x 662Pin LGA |
| 12 | J1 | EXPORT | 1x EXPORT Expansion Connector, 2x20pin Pin Header, 2.0mm Pitch |
| 13 | MIC1 | MIC | 1x 2Pin white terminal block, 2.0mm spacing |
| 14 | J5 | JTAG | 2x 5Pin header，2.54mm spacing |
| 15 | SW1 | BOOT SET | 1x 2bit boot mode selection dip switch |
| 16 | J7 | USB2.0 touch screen interface | 1x 4Pin white terminal block, 2.0mm spacing |
| 17 | J9 | UART | 1x 4Pin white terminal block, 2.0mm spacing |
| 18 | J11 | Debut | 1x 4Pin white terminal block, 2.0mm spacing |
| 19 | J14 | CAN-FD-1 | 1x 4Pin white terminal block, 2.0mm spacing |
| 20 | J16 | CAN-FD-2 | 1x 4Pin white terminal block, 2.0mm spacing |
| 21 | J17 | Capacitive Touch Screen Interface | 1x 6Pin FFC connector, 0.5mm spacing |
| 22 | J18 | USB WiFi | 1x 4Pin Pin Array, 2.0mm Spacing Connects via USB2.0 HOST |
| 23 | J24 | MIPI LCD interface | 1x 40Pin FFC Connector, 0.5mm Spacing |
| 24 | J23 | RGB LCD interface | 1x 40Pin FFC Connector, 0.5mm Spacing |
| 25 | J22 | CAMERA | 1x 30Pin FFC Connector, 0.5mm Spacing |
| 26 | J19 | PoE PD Output | 1x 5Pin Black Row Holder, 2.0mm Spacing |
| 27 | J25 | FRONT | 2x5pin header, 2.0mm spacing |
| 28 | J26 | Micro SIM | 1x 4G Micro SIM card slot |




Development board interface label schematic

## 6.1 Power supply connector（J20）

It is recommended to use a 12V 2A DC power adapter as the power input. For non-12V DC power adapters, please refer to Power Consumption and Power Supply Requirements to select the appropriate power supply.



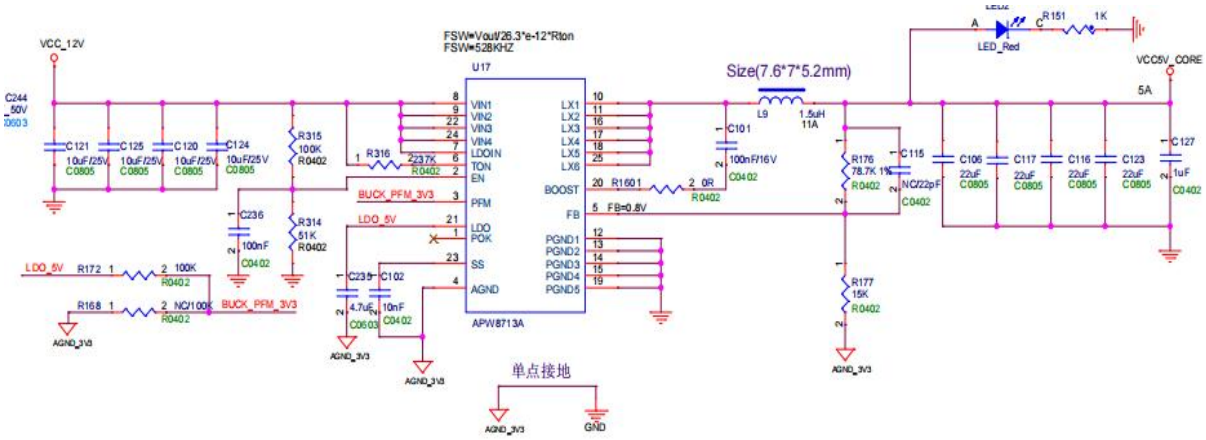

Power supply connector schematic

### 6.1.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J20 | 1 | System power supply input + | 12V | DC Socket ,DC connector Outer diameter 5.5mm, inner diameter 2.1mm |
| | 2 | Power ground | GND | |
| | 3 | Power ground | GND | |

### 6.1.2 Primary conversion circuit

The VIN to 5V recommended circuit is shown in the figure.



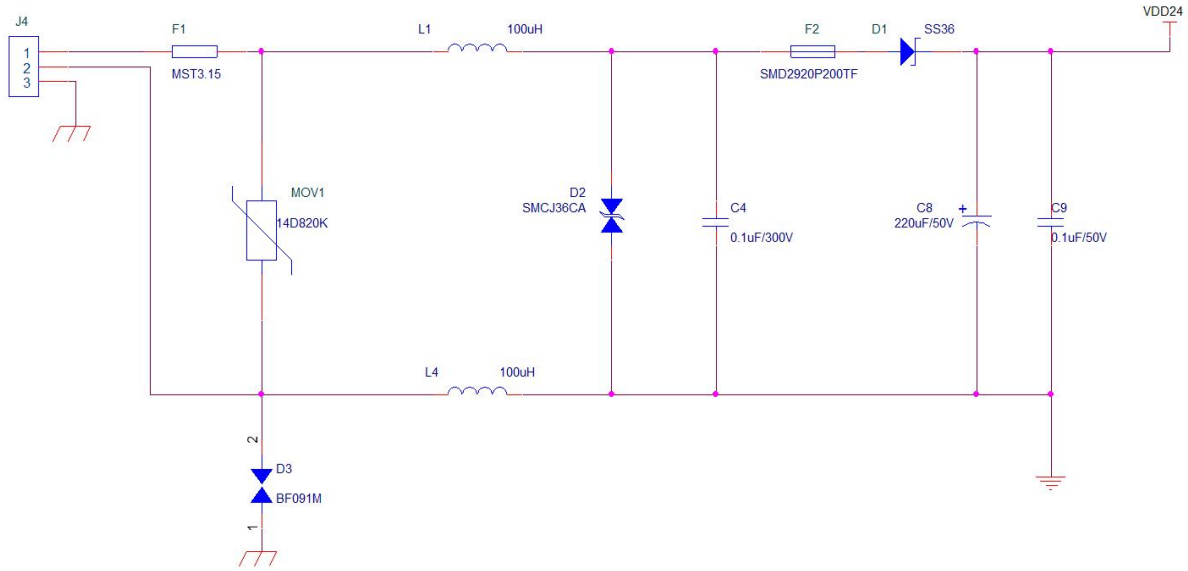

VIN to 5V Recommended Circuit

When the voltage difference between the input and output power supplies is large and the load current is high, the power conversion chip needs to use a DC-DC device with high conversion efficiency, instead of an LDO device, which will burn out the device due to high heat generation.

The reference circuit uses the APW8713A device, which has an input voltage range of 2.7~28V, a maximum output current of 8A, a conversion efficiency of up to 95%, an inductance selectable from 1~4.7uH, and a current rating greater than the load current.

Power Protection Circuit

When the environment in which the equipment is located is harsh, such as when it is placed outdoors and may be subjected to lightning strikes, it is necessary to protect the power supply section. The recommended protection circuit is shown in the figure.



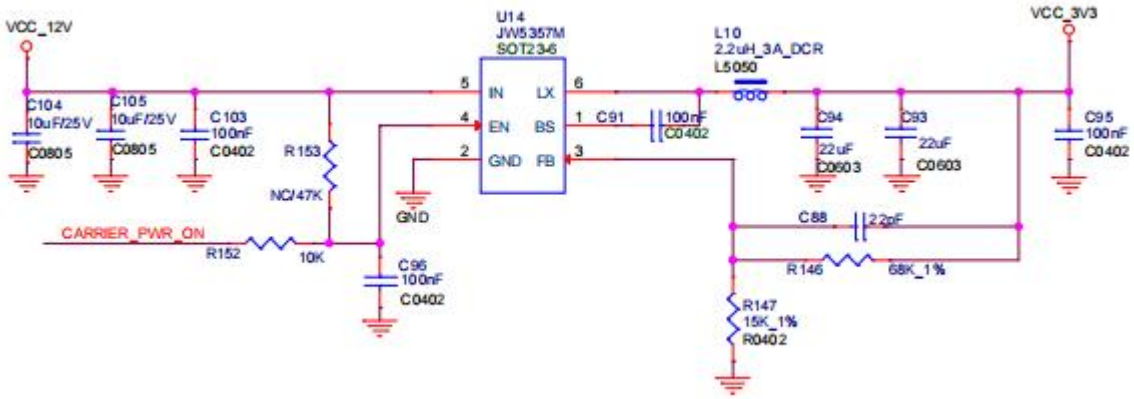

Power supply protection circuit

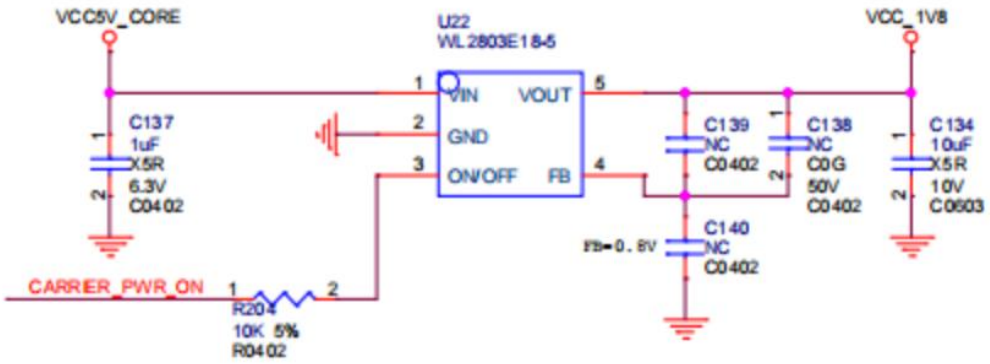
When surge voltage or current occurs in the power port, varistor MOV1 and gas discharge tube D3 form the first level of protection to absorb larger surges. d2 is a TVS tube, mainly for the absorption of residual voltage after the first level of protection. Since the response time of TVS is faster than that of gas discharge tube, in order to prevent TVS from being burnt before the response of gas discharge tube, it is necessary to connect an inductor in series between the two protection circuits to play the effect of time delay.

D1 is a Schottky diode to realize the anti-reverse function.

### 6.1.3 Secondary conversion circuit

Development board other power supply, such as 3.3V, 1.8V, etc., can be obtained by 12V\5V again step-down, the recommended circuit shown in Figure.





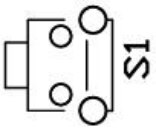

5V to 3.3V circuit

JW5357M is a two-way power conversion device with a maximum output current of 3A and an adjustable output voltage, and the EN pin is connected to the core board. CARRIER_PWR_ON (V17) on. , realizing the timing requirement that the core board is powered up before the base board.

Users can choose other models of power supply devices according to actual needs.

### 6.2 RECOVERY Key(S1)

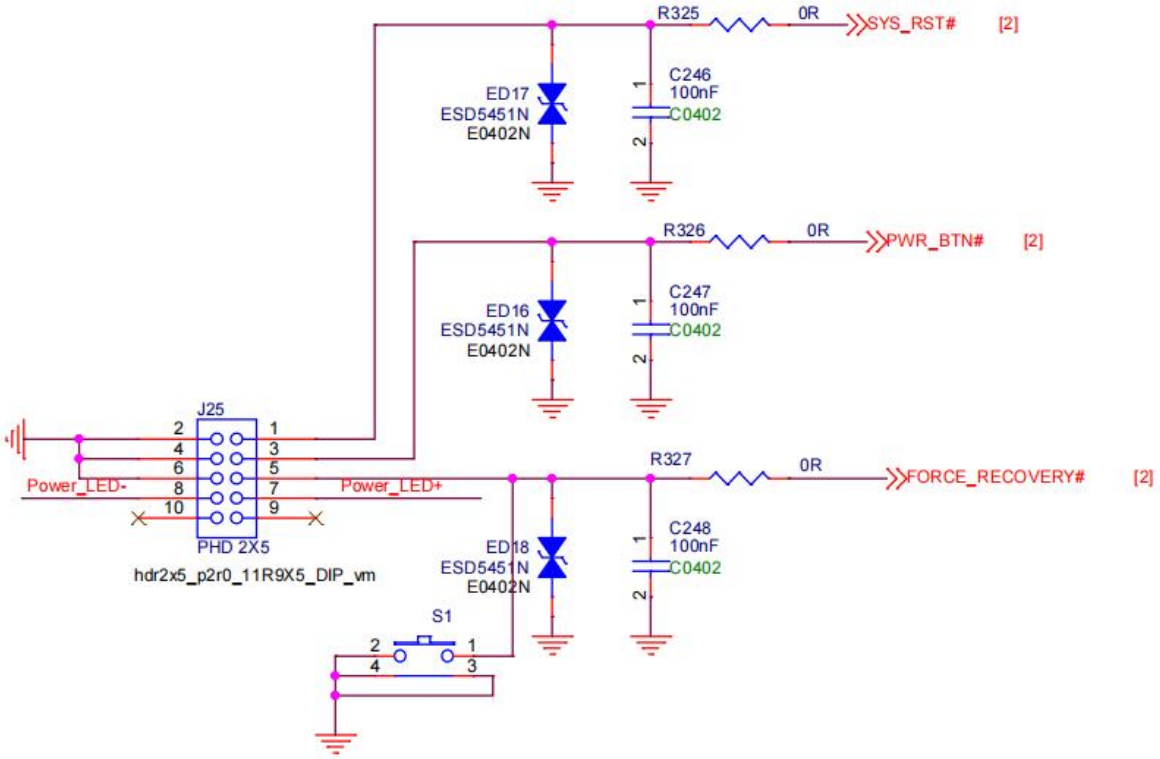
The development board has designed a RECOVERY key for system burning.




Recovery key diagram

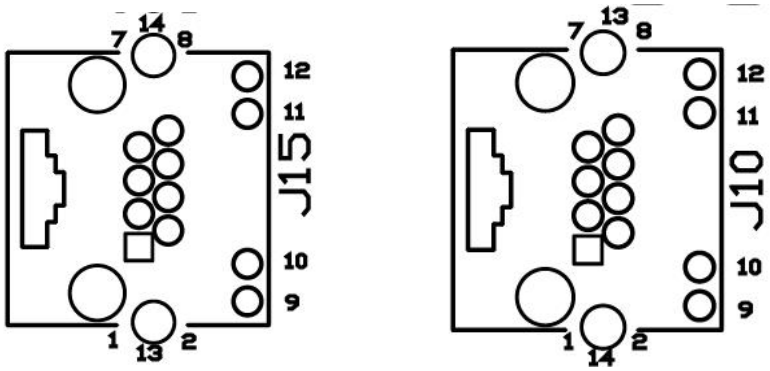
#### 6.2.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| S1 | 1 | Burn mode | REVOVERY | Press the button to enter burn mode |




## 6.3 Ethernet Interface（J15，J10）

Designed with 2 x 1000M Ethernet interface using RJ45 connectors

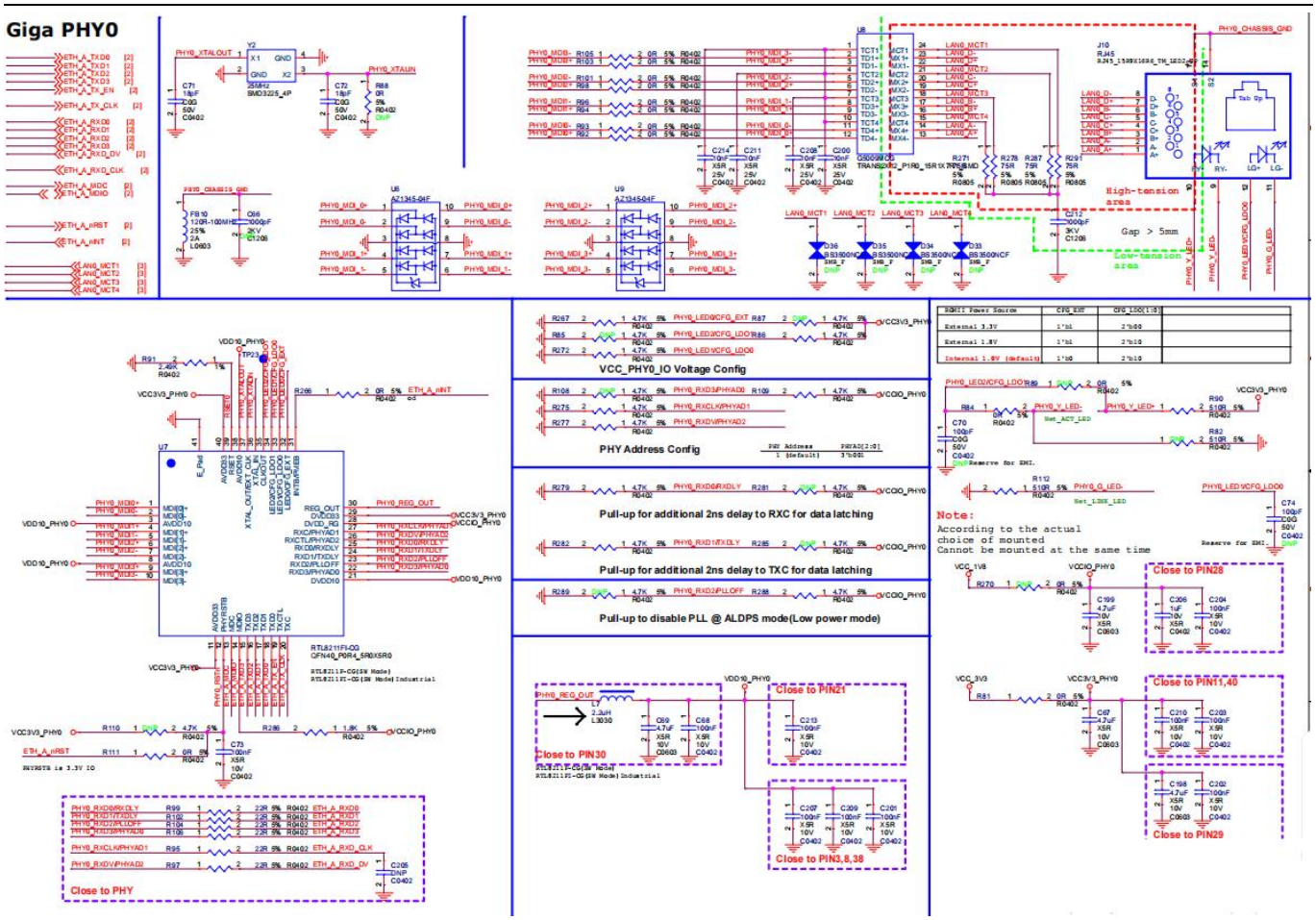


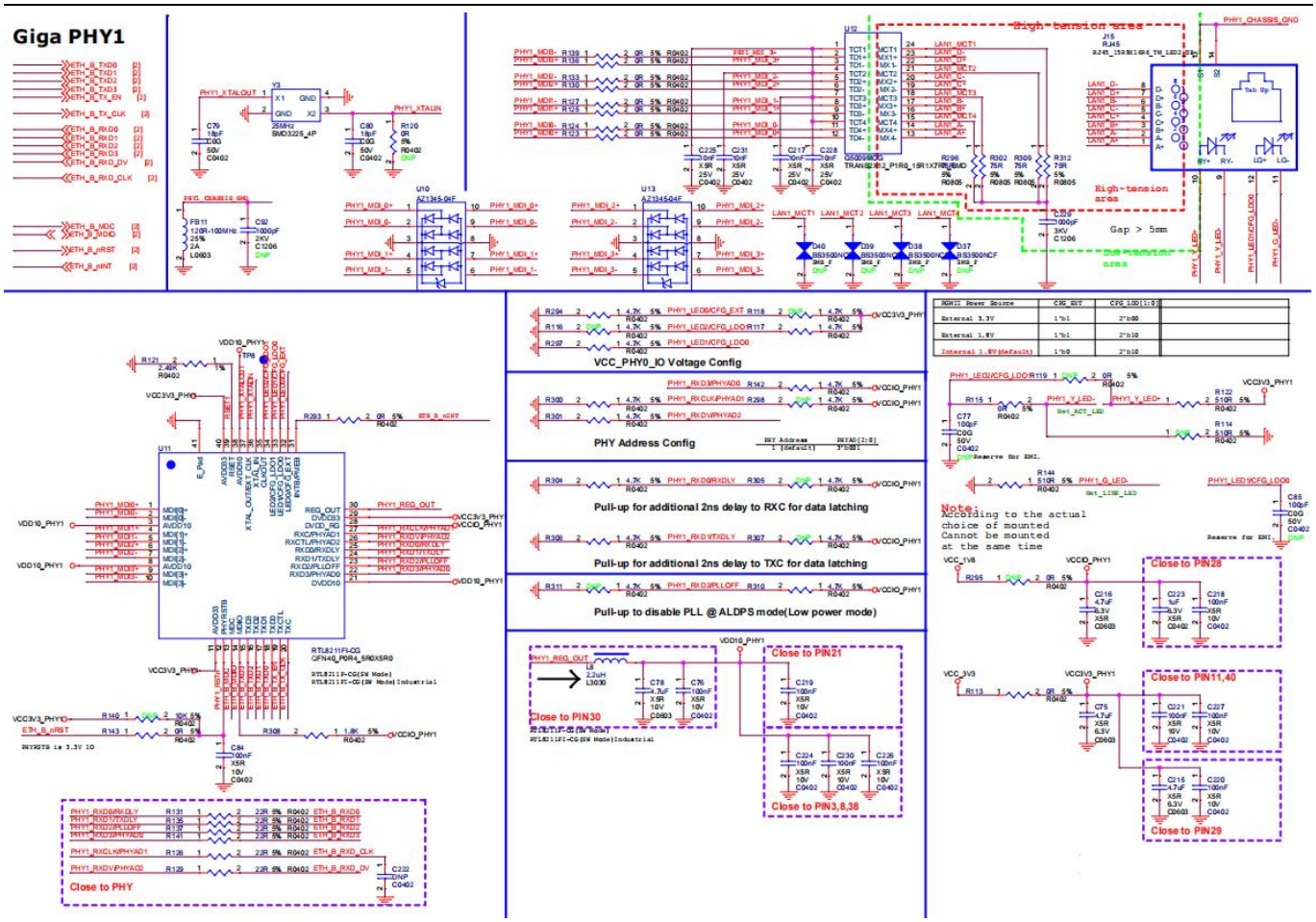

Ethernet interface schematic

### 6.3.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J15 | 1 | ETH_B Differential pairs 0+ | LAN1_A+ | |
| | 2 | ETH_B Differential pairs 0- | LAN1_A- | |
| | 3 | ETH_B Differential pairs 1+ | LAN1_B+ | |

| | | | | |
|---|---|---|---|---|
| | 4 | ETH_B Differential pairs 1- | LAN1_B- | |
| | 5 | ETH_B Differential pairs 2+ | LAN1_C+ | |
| | 6 | ETH_B Differential pairs 2- | LAN1_C- | |
| | 7 | ETH_B Differential pairs 3+ | LAN1_D+ | |
| | 8 | ETH_B Differential pairs 3- | LAN1_D- | |
| | 9 | Power ground | PHY1_Y_LED- | |
| | 10 | LINK Yellow LED | PHY1_Y_LED+ | |
| | 11 | Power ground | PHY1_G_LED- | |
| | 12 | LINK Green LED | PHY1_LED1/CFG_LDO0 | |
| | 13 | Shell ground | GND | |
| | 14 | Shell ground | GND | |
| J10 | 1 | ETH_A Differential pairs 0+ | LAN0_A+ | |
| | 2 | ETH_A Differential pairs 0- | LAN0_A- | |
| | 3 | ETH_A Differential pairs 1+ | LAN0_B+ | |
| | 4 | ETH_A Differential pairs 1- | LAN0_B- | |
| | 5 | ETH_A Differential pairs 2+ | LAN0_C+ | |
| | 6 | ETH_A Differential pairs 2- | LAN0_C- | |
| | 7 | ETH_A Differential pairs 3+ | LAN0_D+ | |
| | 8 | ETH_A Differential pairs 3- | LAN0_D- | |
| | 9 | Power ground | PHY0_Y_LED- | |
| | 10 | LINK Yellow LED | PHY0_Y_LED+ | |
| | 11 | Power ground | PHY0_G_LED- | |
| | 12 | LINK Green LED | PHY0_LED1/CFG_LDO0 | |
| | 13 | Shell ground | GND | |
| | 14 | Shell ground | GND | |


Giga PHY0
High-tension area
Gap > 5mm
Low-tension area
VCC_PHY0_IO Voltage Config
PHY Address Config
Pull-up for additional 2ns delay to RXC for data latching
Pull-up for additional 2ns delay to TXC for data latching
Pull-up to disable PLL @ ALDPS mode(Low power mode)
Note:
According to the actual choice of mounted
Cannot be mounted at the same time
Close to PIN28
Close to PIN11,40
Close to PIN29
Close to PIN21
Close to PIN30
Close to PIN3,8,38
Close to PHY

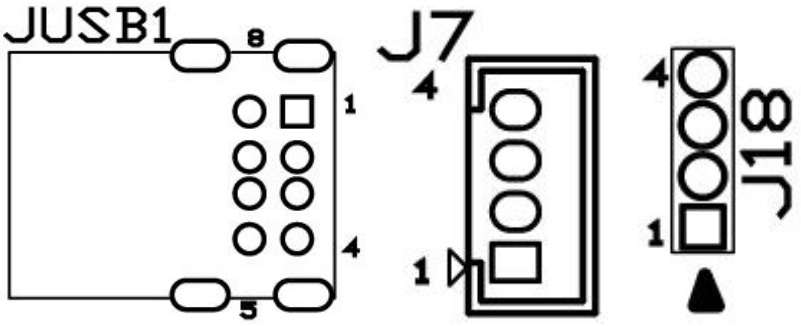



### 6.3.2 Performance

| Parameter | Test method | Min | Typical | Max | Unit | Test Command |
|---|---|---|---|---|---|---|
| TCP Mode speed | Iperf3 | - | 913 | - | Mb/s | Client receive： iperf3 -c x.x.x.x -i 2 -t 60 |
| | Iperf3 | - | 913 | - | Mb/s | Client transmit： iperf3 -c x.x.x.x -i 2 -t 60 -R |
| UDP Mode speed | Iperf3 | - | 920 | - | Mb/s | client：iperf3 -c 192.168.x.x -t 20 -i 2 -u -b 1000M |

## 6.4 USB Interface（JUSB1、J7、J18）

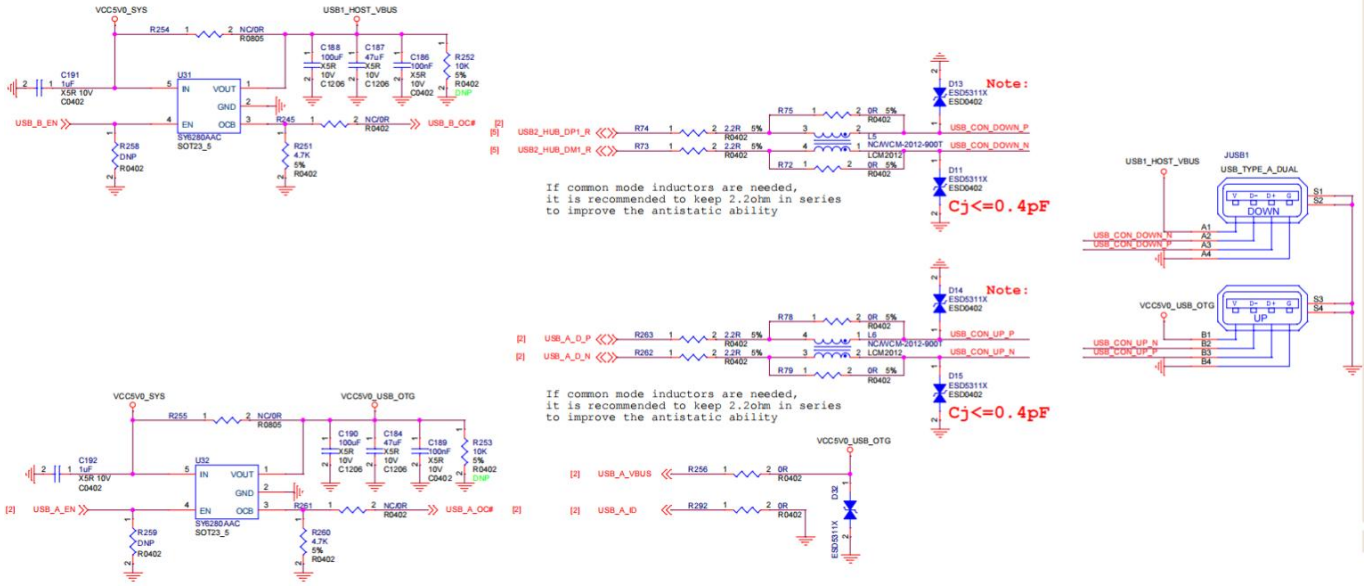
Four USB HOST and one USB OTG interfaces are designed, including one USB HOST and one USB OTG with Type A interface, and the other three USB HOST are used for USB touch screen interface, USB WiFi module and Mini PCIe interface (connecting 4G module).



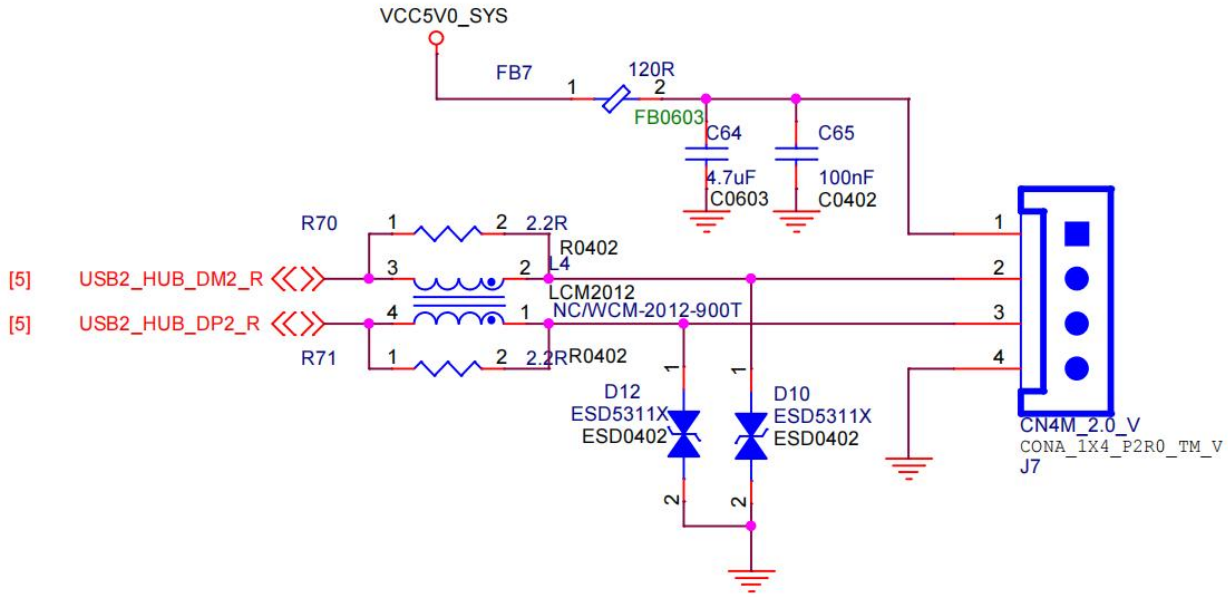

USB2.0 interface schematic

### 6.4.1 Pin Definitions

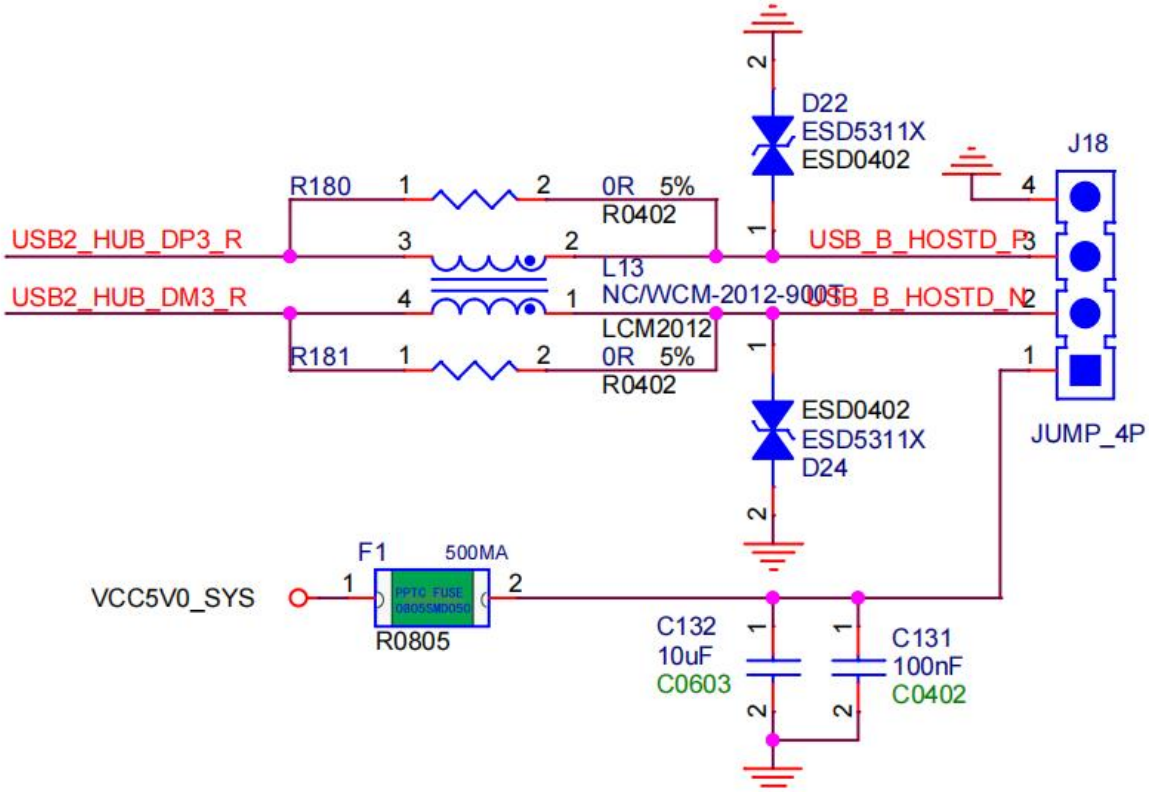
| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| JUSB1 down | 1 | USB 5V power supply | USB1_HOST_VBUS 5V | 5V |
| | 2 | USB HOST 1 data - | USB_CON_DOWN_N | USB HOST 1 |
| | 3 | USB HOST 1 data + | USB_CON_DOWN_P | |
| | 4 | Ground signal | GND | |
| JUSB1 up | 1 | USB 5V power supply | VCC5V0_USB_OTG 5V | |
| | 2 | USB_A_OTG data - | USB_CON_UP_N | USB_A_OTG |
| | 3 | USB_A_OTG data + | USB_CON_UP_P | |
| | 4 | Ground signal | GND | |
| J7 | 1 | USB 5V power supply | VCC5V0_SYS | 5V |
| | 2 | USB HOST 2 data - | USB2_HUB_DM2 | USB Touch Screen |
| | 3 | USB HOST 2 data + | USB2_HUB_DP2 | |
| | 4 | Ground signal | GND | |
| J18 | 1 | USB 5V power supply | VCC5V0_SYS | 5V |
| | 2 | USB HOST 3 data - | USB2_HUB_DM3 | USB WiFi Module |
| | 3 | USB HOST 3 data + | USB2_HUB_DP3 | |
| | 4 | Ground signal | GND | |




## Touch Panel connector

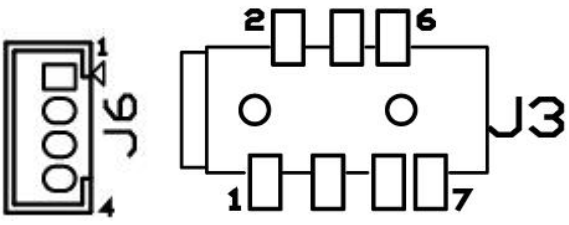


# WIFI/BT




### 6.5 AUDIIO Interface（J6、J3）

Designed to have a 3.5mm standard headphone jack J3 for evaluating audio-related features, the J6 is reserved for speaker output holders.



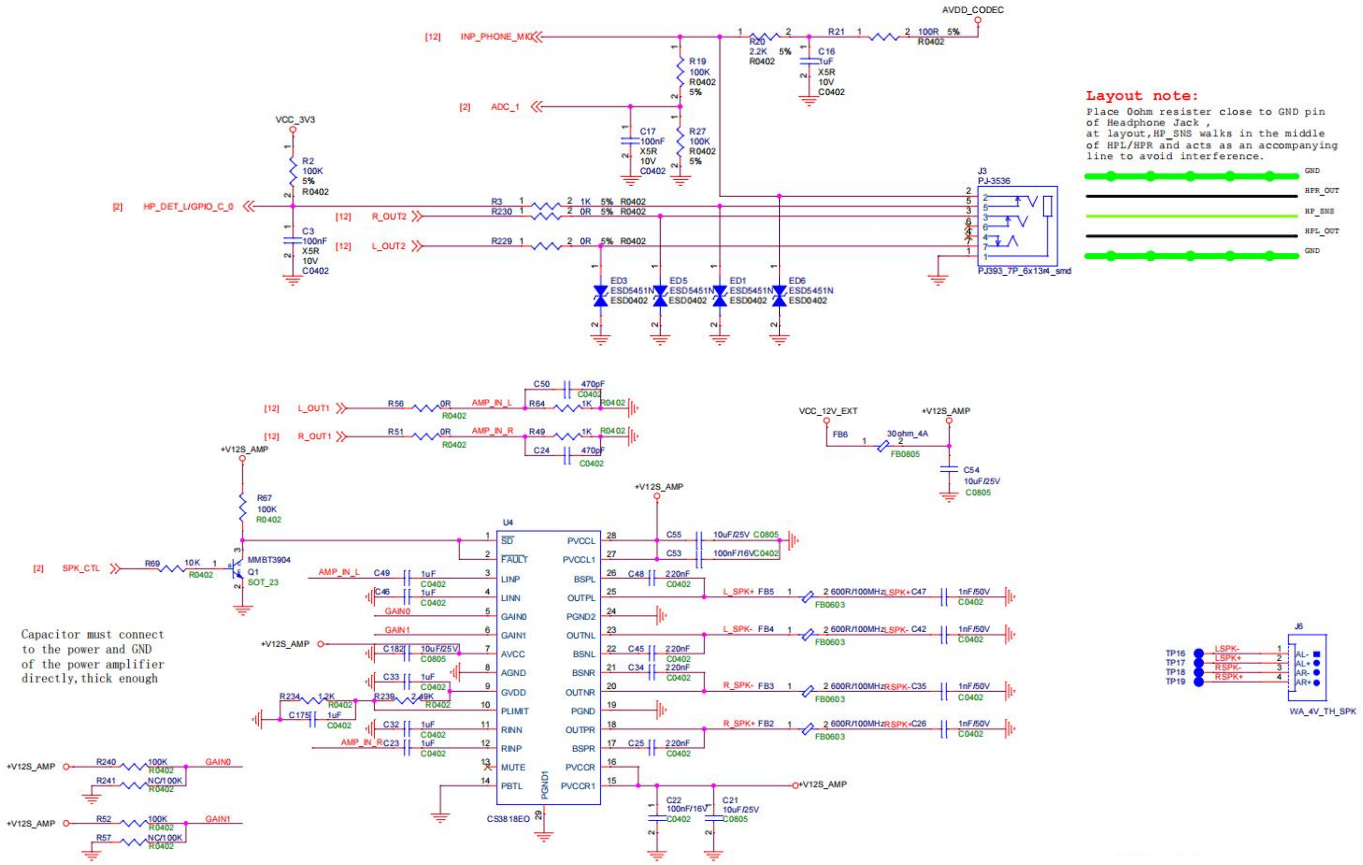

Audio interface schematic

#### 6.5.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J6 | 1 | Speaker left channel data - | LSPK- | |
| | 2 | Speaker left channel data+ | LSPK+ | |

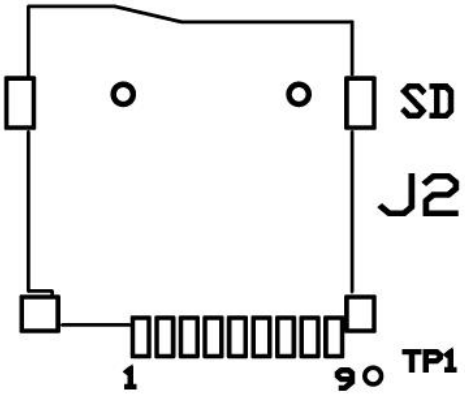
| | | | | |
|---|---|---|---|---|
| | 3 | Speaker right channel data- | RSPK- | |
| | 4 | Speaker right channel data+ | RSPK+ | |
| J3 | 1 | Ground signal | GND | |
| | 2 | Microphone input | INP_PHONE_MIC | |
| | 3 | Right sound output | R_OUT2 | |
| | 4 | NC | NC | |
| | 5 | Output detection signal | HP_DET_L/GPIO_C_0 | |
| | 6 | NC | NC | |
| | 7 | Left sound output | L_OUT2 | |

**Headphone Jack(4-pole with DET & MIC)**




## 6.6 SD Card Interface（J2）

The development board designs a Micro SD card slot circuit that can be used for system startup, burning, and storage.

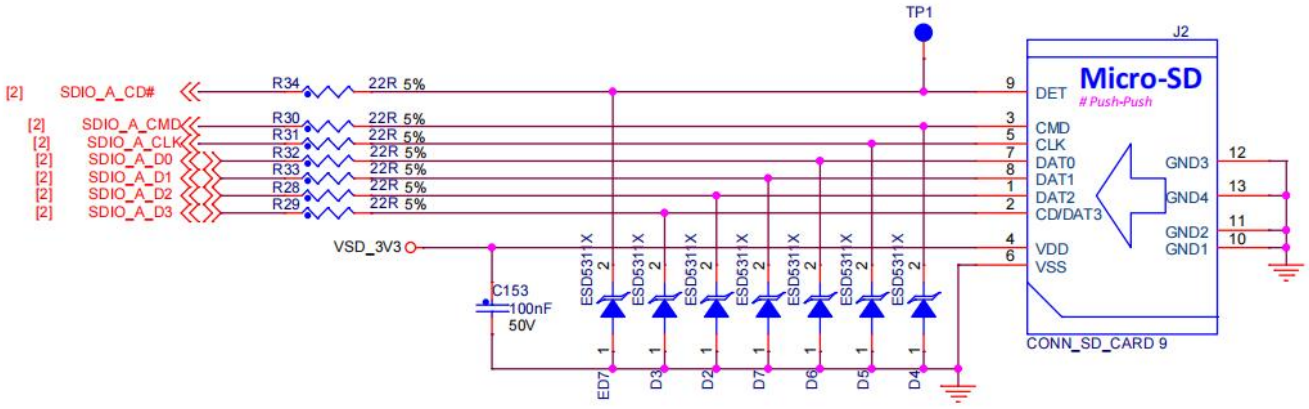


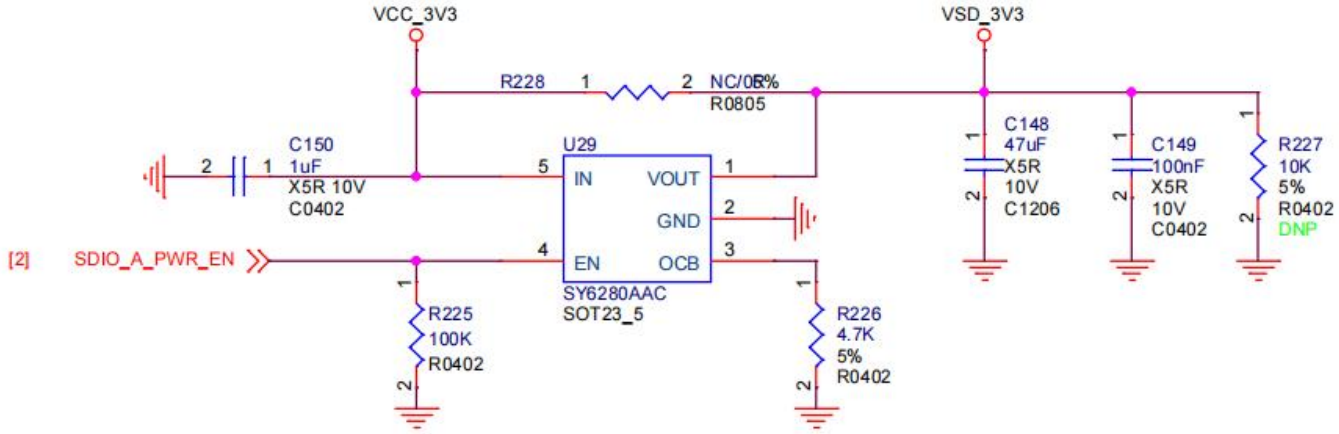

Micro SD Card schematic

### 6.6.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J2 | 1 | SDIO_A data 2 | SDIO_A_D2 | |
| | 2 | SDIO_A data 3 | SDIO_A_D3 | |
| | 3 | SDIO_A command | SDIO_A_CMD | |
| | 4 | Power supply 3.3V | VSD_3V3 | |
| | 5 | SDIO_A clocks | SDIO_A_CLK | |
| | 6 | Ground signal | GND | |
| | 7 | SDIO_A data 0 | SDIO_A_D0 | |
| | 8 | SDIO_A data 1 | SDIO_A_D1 | |
| | 9 | Plug-in card detection | SDIO_A_CD | |
| | 10 | Shell ground | GND | |
| | 11 | Shell ground | GND | |
| | 12 | Shell ground | GND | |
| | 13 | Shell ground | GND | |

In the debugging process, it is often necessary to carry out program upgrade operations, therefore, it is necessary to add a TF card interface on the development board, the circuit is shown in Figure.

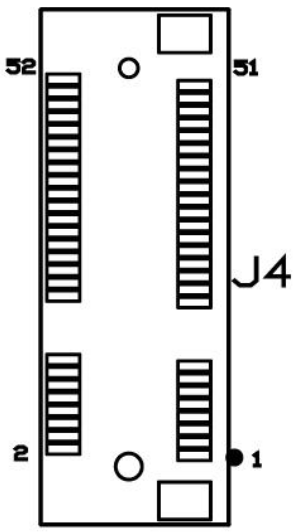





It is recommended to pull up all signals, when PCB wiring, DAT[3:0] and CLK signals need to be processed with equal length, the error is recommended to be 50mil Inside.

### 6.7 Mini PCIe Interface（J4）

Provides 1 Mini PCIe interface to support single USB2.0 devices



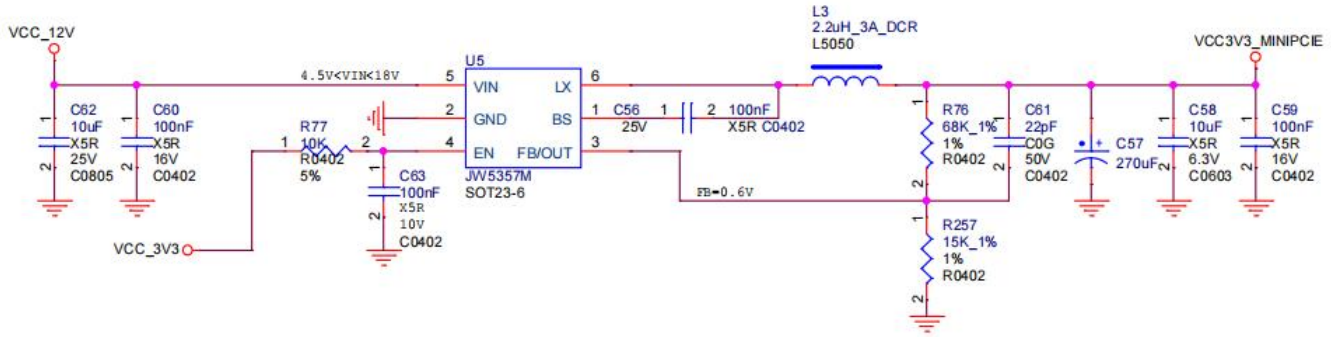

Mini PCIe 接口示意图

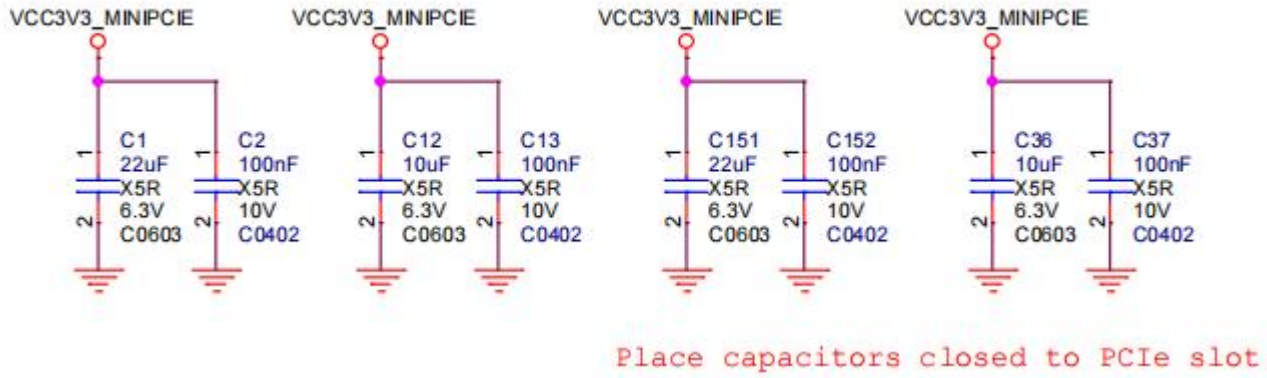
#### 6.7.1 Pin Definitions

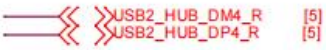
| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J4 | 1 | NC | NC | |
| | 2 | Power supply 3.3V | VCC3V3_MINIPCIE | |
| | 3 | NC | NC | |

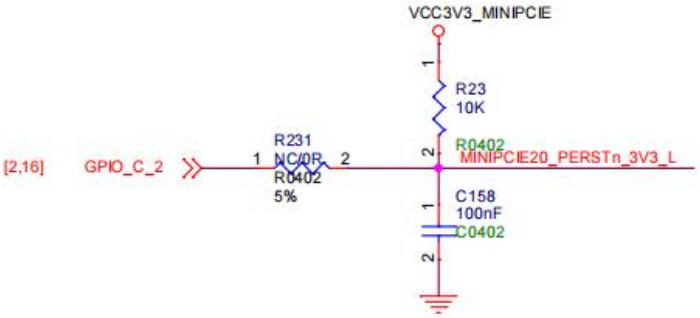
| | | | | |
|---|---|---|---|---|
| | 4 | Ground signal | GND | |
| | 5 | NC | NC | |
| | 6 | NC | NC | |
| | 7 | NC | NC | |
| | 8 | SIM card power supply | UIM_PWR | |
| | 9 | Ground signal | GND | |
| | 10 | SIM card data signal | UIM_DATA | |
| | 11 | NC | NC | |
| | 12 | SIM card clock | UIM_CLK | |
| | 13 | NC | NC | |
| | 14 | SIM card reset | UIM_RESET | |
| | 15 | Ground signal | GND | |
| | 16 | NC | NC | |
| | 17 | NC | NC | |
| | 18 | Ground signal | GND | |
| | 19 | NC | NC | |
| | 20 | NC | NC | |
| | 21 | Ground signal | GND | |
| | 22 | MiniPCIe reset | MINIPCIE20_PERSTn_3V3_L | |
| | 23 | NC | NC | |
| | 24 | Power supply 3.3V | VCC3V3_MINIPCIE | |
| | 25 | NC | NC | |
| | 26 | Ground signal | GND | |
| | 27 | 地信号 | GND | |
| | 28 | NC | NC | |
| | 29 | Ground signal | GND | |
| | 30 | NC | NC | |
| | 31 | NC | NC | |

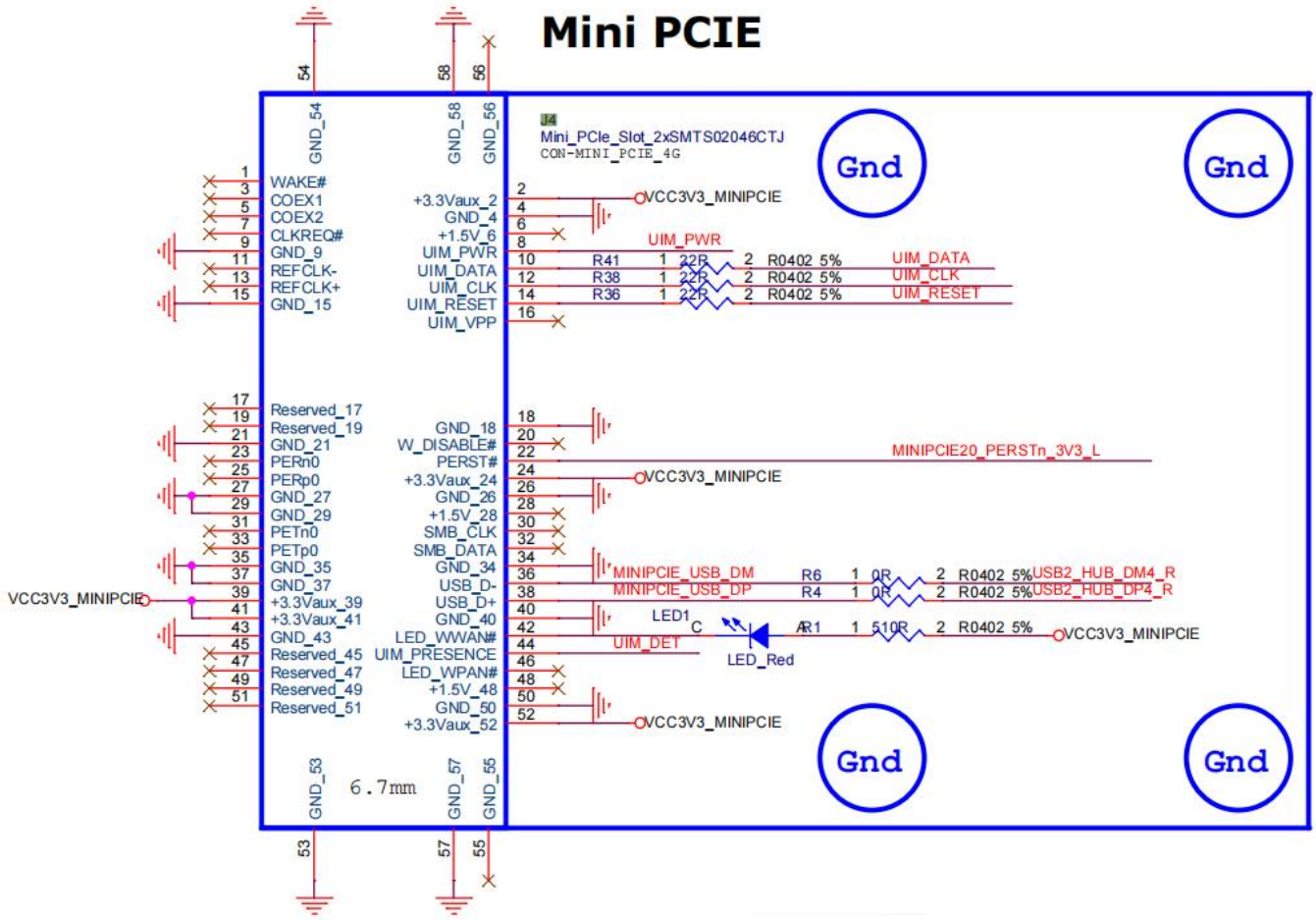
| | | | | |
|---|---|---|---|---|
| | 32 | NC | NC | |
| | 33 | NC | NC | |
| | 34 | Ground signal | GND | |
| | 35 | Ground signal | GND | |
| | 36 | USB2.0 HUB 4 data - | MINI_PCIE_USB_DM | USB2_HUB_DM4 |
| | 37 | Ground signal | GND | |
| | 38 | USB2.0 HUB 4 data + | MINI_PCIE_USB_DP | USB2_HUB_DP4 |
| | 39 | Power supply 3.3V | VCC3V3_MINIPCIE | |
| | 40 | Ground signal | GND | |
| | 41 | Power supply 3.3V | VCC3V3_MINIPCIE | |
| | 42 | LED power supply | LED_WWAN | |
| | 43 | Ground signal | GND | |
| | 44 | SIM card detection signal | UIM_DET | |
| | 45 | NC | NC | |
| | 46 | NC | NC | |
| | 47 | NC | NC | |
| | 48 | NC | NC | |
| | 49 | NC | NC | |
| | 50 | Ground signal | GND | |
| | 51 | NC | NC | |
| | 52 | Power supply 3.3V | VCC3V3_MINIPCIE | |

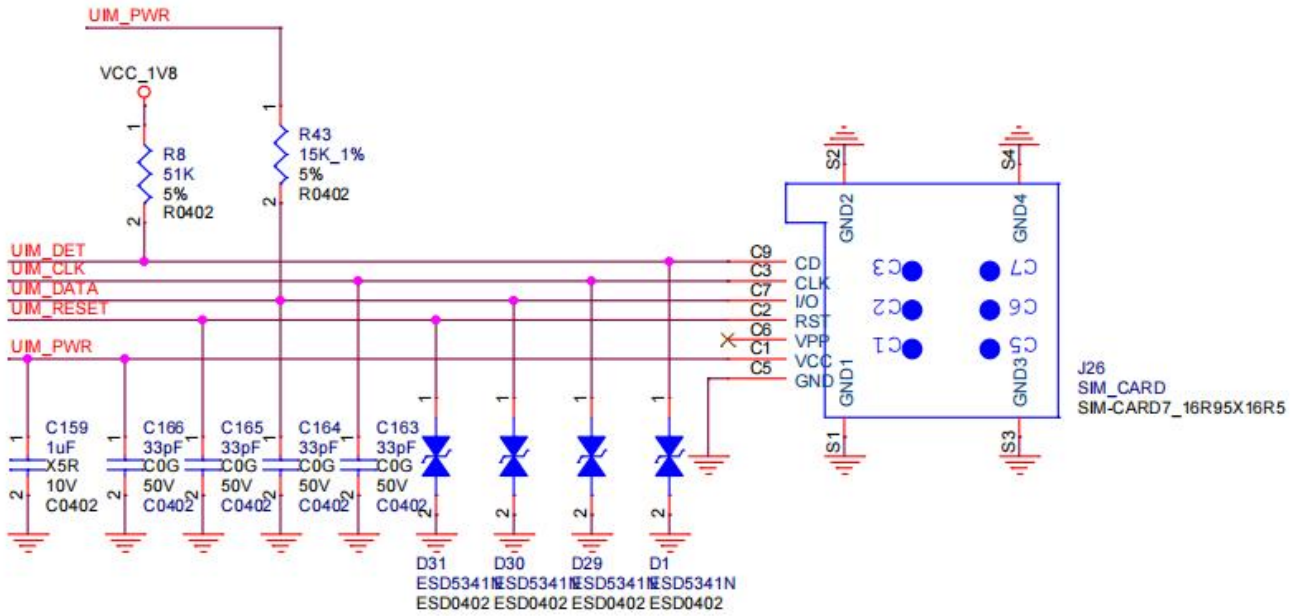



VCC3V3_MINIPCIE
C1
22uF
X5R
6.3V
C0603
C2
100nF
X5R
10V
C0402
VCC3V3_MINIPCIE
C12
10uF
X5R
6.3V
C0603
C13
100nF
X5R
10V
C0402
VCC3V3_MINIPCIE
C151
22uF
X5R
6.3V
C0603
C152
100nF
X5R
10V
C0402
VCC3V3_MINIPCIE
C36
10uF
X5R
6.3V
C0603
C37
100nF
X5R
10V
C0402
Place capacitors closed to PCIe slot


USB2_HUB_DM4_R [5]
USB2_HUB_DP4_R [5]

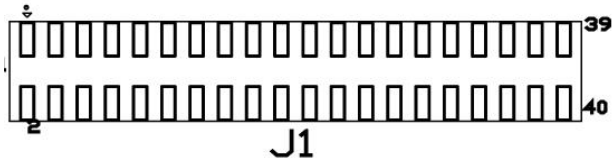

VCC3V3_MINIPCIE
R23
10K
[2,16]
GPIO_C_2
R231
NC/0R
R0402
5%
R0402
MINIPCIE20_PERSTn_3V3_L
C158
100nF
C0402


Mini PCIE
J4
Mini_PCIe_Slot_2xSMTS02046CTJ
CON-MINI_PCIE_4G
Gnd
Gnd
Gnd
Gnd
WAKE#
COEX1
COEX2
CLKREQ#
GND_9
REFCLK-
REFCLK+
GND_15
+3.3Vaux_2
GND_4
+1.5V_6
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
VCC3V3_MINIPCIE
R41 22R R0402 5%
R38 22R R0402 5%
R36 22R R0402 5%
Reserved_17
Reserved_19
GND_21
PERn0
PERp0
GND_27
GND_29
PETn0
PETp0
GND_35
GND_37
+3.3Vaux_39
+3.3Vaux_41
GND_43
Reserved_45
Reserved_47
Reserved_49
Reserved_51
GND_18
W_DISABLE#
PERST#
+3.3Vaux_24
GND_26
+1.5V_28
SMB_CLK
SMB_DATA
GND_34
USB_D-
USB_D+
GND_40
LED_WWAN#
UIM_PRESENCE
LED_WPAN#
+1.5V_48
GND_50
+3.3Vaux_52
MINIPCIE20_PERSTn_3V3_L
MINIPCIE_USB_DM
MINIPCIE_USB_DP
R6 0R R0402 5%
R4 0R R0402 5%
USB2_HUB_DM4_R
USB2_HUB_DP4_R
LED1
LED_Red
R1 510R R0402 5%
6.7mm


UIM_PWR
VCC_1V8
R8 51K 5% R0402
R43 15K_1% 5% R0402
UIM_DET
UIM_CLK
UIM_DATA
UIM_RESET
C159 1uF X5R 10V C0402
C166 33pF C0G 50V C0402
C165 33pF C0G 50V C0402
C164 33pF C0G 50V C0402
C163 33pF C0G 50V C0402
D31 ESD5341N ESD0402
D30 ESD5341N ESD0402
D29 ESD5341N ESD0402
D1 ESD5341N ESD0402
C9 CD
C3 CLK
C7 I/O
C2 RST
C6 VPP
C1 VCC
C5 GND
J26
SIM_CARD
SIM-CARD7_16R95X16R5

## 6.8 GPIO/QSPI/UART/I2C Interface（J1）

A 2.0-spacing 40 PIN twin row needle was designed on which 5V power supply, 3.3V power supply, 4*UART, 1*QSPI, 1*SPI,1*I2C and several GPIO signals were defined.

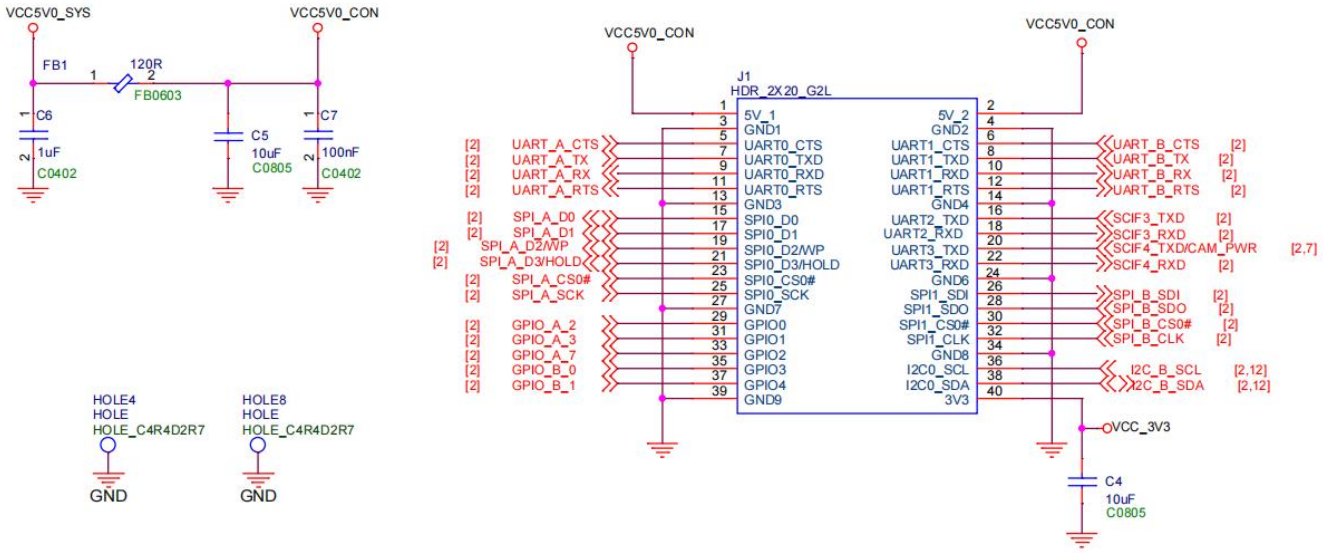



GPIO/QSPI/UART/I2C interface schematics

### 6.8.1 Pin Definitions

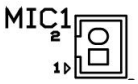
| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J1 | 1 | Output power supply 5V | VCC5V0_CON | |
| | 2 | Output power supply5V | VCC5V0_CON | |
| | 3 | Ground signal | GND | |
| | 4 | Ground signal | GND | |
| | 5 | UART_A Clear to send | UART_A_CTS | |
| | 6 | UART_B Clear to send | UART_B_CTS | |
| | 7 | UART_A send data | UART_A_TX | |
| | 8 | UART_B send data | UART_B_TX | |
| | 9 | UART_A receive data | UART_A_RX | |
| | 10 | UART_B receive data | UART_B_RX | |
| | 11 | UART_A Request to send | UART_A_RTS | |
| | 12 | UART_B Request to send | UART_B_RTS | |
| | 13 | Ground signal | GND | |
| | 14 | Ground signal | GND | |
| | 15 | QSPI_A data 0 | SPI_A_D0 | |
| | 16 | UART3 send data | SCIF3_TXD | |
| | 17 | QSPI_A Data input output 1/Data output | SPI_A_D1 | |
| | 18 | UART3 receive data | SCIF3_RXD | |
| | 19 | QSPI_A Data input output 2/Write protect input | SPI_A_D2/WP | |

| | | | | |
|---|---|---|---|---|
| | 20 | UART4 send data | SCIF4_TXD/CAN_PWR | |
| | 21 | QSPI_A Data input output 3/Hold or Reset input | SPI_A_D3/HOLD | |
| | 22 | UART4 receive data | SCIF4_RXD | |
| | 23 | QSPI_A Chip select input | SPI_A_CS0 | |
| | 24 | Ground signal | GND | |
| | 25 | QSPI_A clock | SPI_A_SCK | |
| | 26 | SPI_B Master out slave in | SPI_B_SDI(MOSI) | |
| | 27 | Ground signal | GND | |
| | 28 | SPI_B Master in slave out | SPI_B_SDO(MISO) | |
| | 29 | GPIO | GPIO_A_2 | |
| | 30 | SPI_B Chip select input | SPI_B_CS0 | |
| | 31 | GPIO | GPIO_A_3 | |
| | 32 | SPI_B synchronous clock signal | SPI_B_CLK | |
| | 33 | GPIO | GPIO_A_7 | |
| | 34 | Ground signal | GND | |
| | 35 | GPIO | GPIO_B_0 | |
| | 36 | I2C_B clock | I2C_B_SCL | |
| | 37 | GPIO | GPIO_B_1 | |
| | 38 | I2C_B data | I2C_B_SDA | |
| | 39 | Ground signal | GND | |
| | 40 | Output power supply 3.3V | VCC_3V3 | |




## 6.9 Microphone Interface (MIC1)

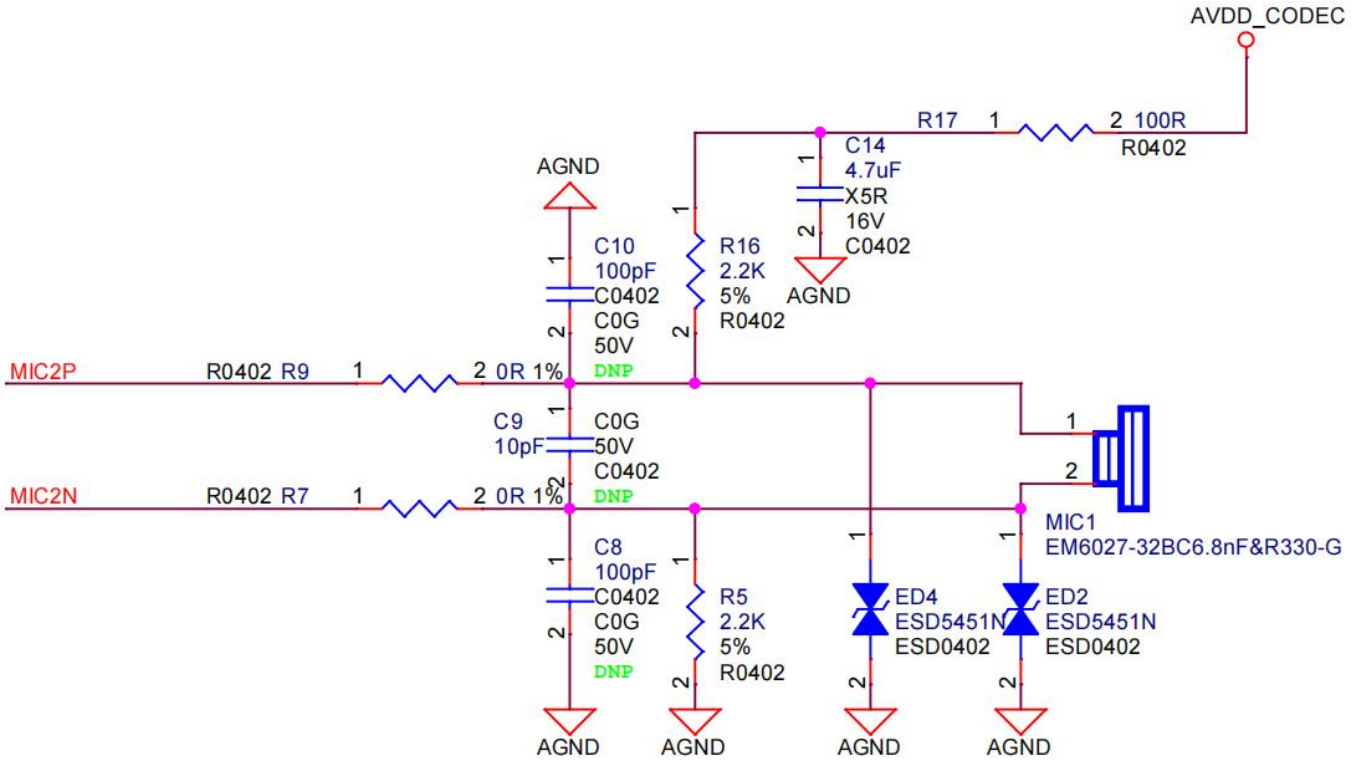
Design of the road microphone interface




Microphone connector schematic

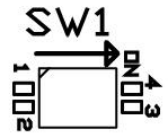
### 6.9.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| MIC1 | 1 | Microphone input signal+ | MIC2P | EM6027-32BC6.8nF&R330-G |
| | 2 | Microphone input signal- | MIC2N | |




### 6.10 BOOT Switch

Designed 2-bit dip switch.




BOOT dip switch schematic

The G2L processor supports the following boot methods.

| MD_BOOT2 to MD_BOOT0 | | | Boot Mode | Interface Module | Connected Device |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Boot mode 0 | SDHI0 | eSD (3.3 V at startup) |
| 0 | 0 | 1 | Boot mode 1 | SDHI0 | 1.8-V eMMC |
| 0 | 1 | 0 | Boot mode 2 | SDHI0 | 3.3-V eMMC |
| 0 | 1 | 1 | Boot mode 3 | SPIBSC | 1.8-V Single, Quad, or Octal serial flash memory |
| 1 | 0 | 0 | Boot mode 4 | SPIBSC | 3.3-V Single or Quad serial flash memory |
| 1 | 0 | 1 | Boot mode 5 | SCIF0 | Downloading through SCIF |
| 1 | 1 | 0 | Reserved | — | Reserved |
| 1 | 1 | 1 | Reserved | — | Reserved |

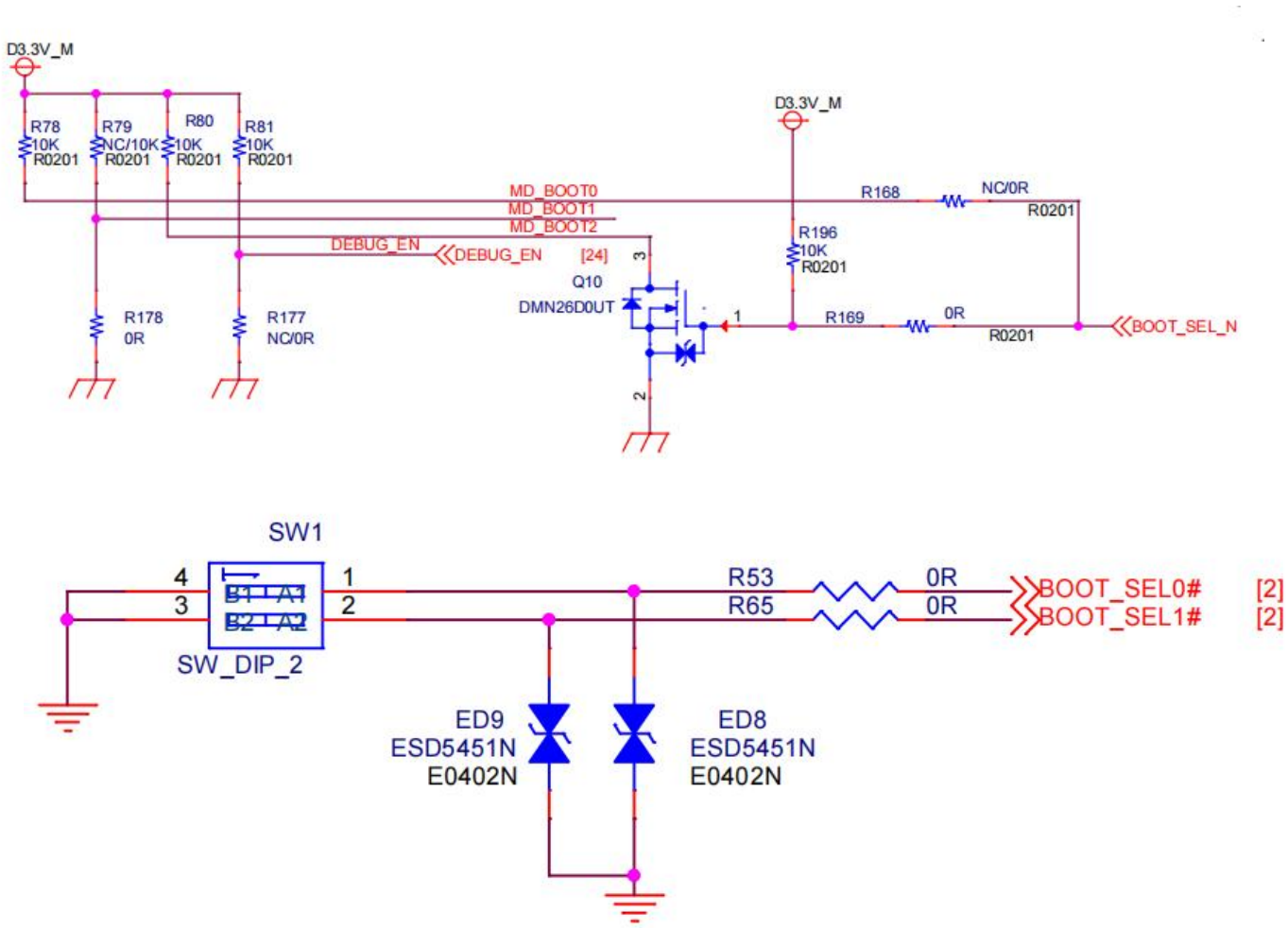
#### 6.10.1 Boot mode description

1)The core board SDHI0 is equipped with an eMMC device, which does not support eSD card startup at the moment.

2) The default level of eMMC on the core board is 1.8V.

3) The core board is equipped with SPI device, the default boot from SPI flash.

In order to support different boot modes, it is necessary to pull up and down the BOOT pin on the base board, the circuit diagram is shown below.




BOOT pin configuration circuit

BOOT_SEL0# of SW1 corresponds to BOOT_SET_N of the core board, and BOOT_SEL1# is empty.

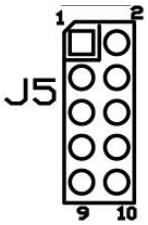
The currently supported boot mode are configured as shown in the following table.

| SW1 Status | Boot mode |
|---|---|
| 01 | eMMC |
| 11 | Serial port |

Note: 0 indicates SW1 ends are disconnected; 1 identifies SW1 ends are shorted.

### 6.11 JTAG Interface（J5）

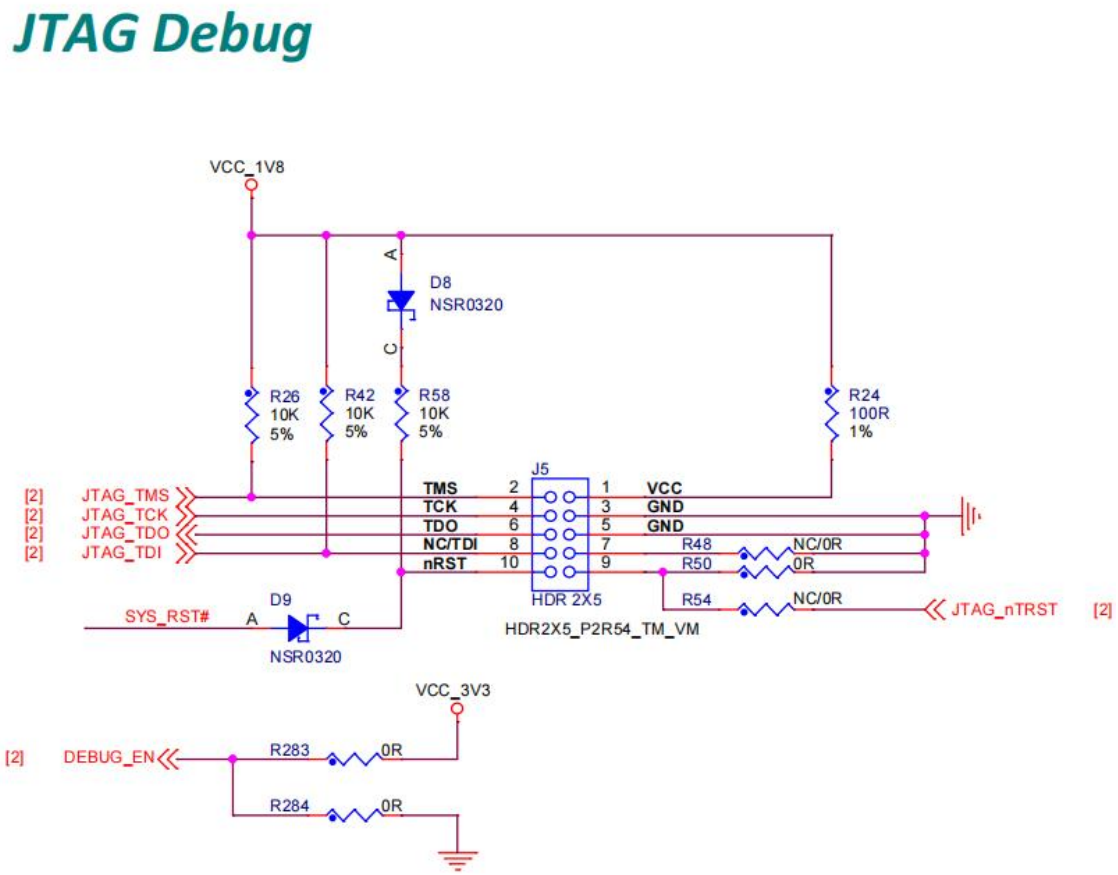
A JTAG interface is reserved for system debugging.




JTAG interface schematic

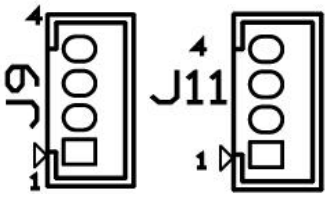
### 6.11.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J5 | 1 | Power supply 1.8V | VCC | 1.8V |
| | 2 | Mode selection signal | JTAG_TMS | |
| | 3 | Ground signal | GND | |
| | 4 | Time cycle clock | JTAG_TCK | |
| | 5 | Ground signal | GND | |
| | 6 | Data output signal | JTAG_TDO | |
| | 7 | NC | NC | |
| | 8 | Test data input | JTAG_TDI | |
| | 9 | Ground signal | GND | |
| | 10 | System Reset | SYS_RST# | |



## 6.12 UART Serial Interface（J9、J11）

Two UART serial ports are designed for debugging the system A55 core and M33 core.

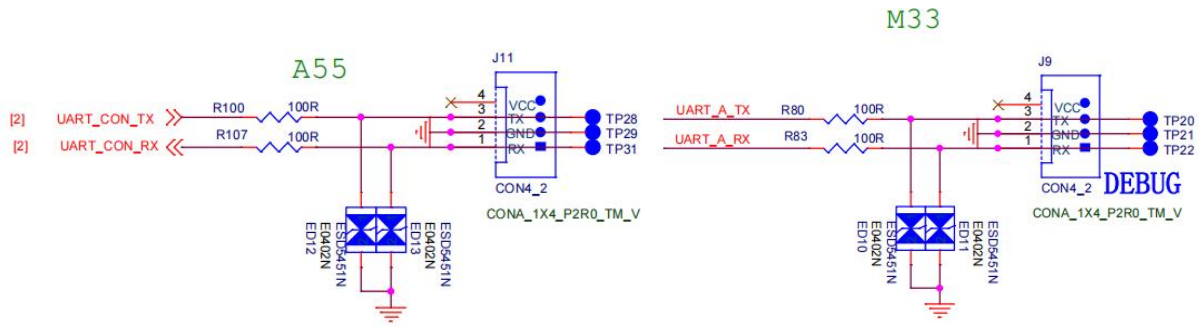



UART serial port schematic

### 6.12.1 Pin Definitions

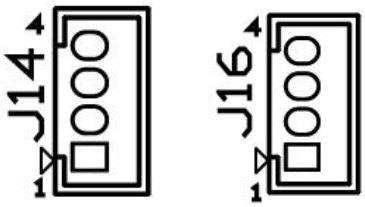
| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J9 | 1 | NC | NC | M33 core debugging serial port |
| | 2 | UART_A send data | UART_A_TX | |
| | 3 | Ground signal | GND | |
| | 4 | UART_A receive data | UART_A_RX | |
| J11 | 1 | NC | NC | A55 core debugging serial port |
| | 2 | UART_CON send data | UART_CON_TX | |
| | 3 | Ground signal | GND | |
| | 4 | UART_CON receive data | UART_CON_RX | |

The DB-G2L V2 can only be used for program burning and system debugging through the SCIF0(UART_CON) serial port, so the interface must be pinned out on the backplane, and the interface circuit is shown in the figure.



## 6.13 CAN Interface（J14，J16）

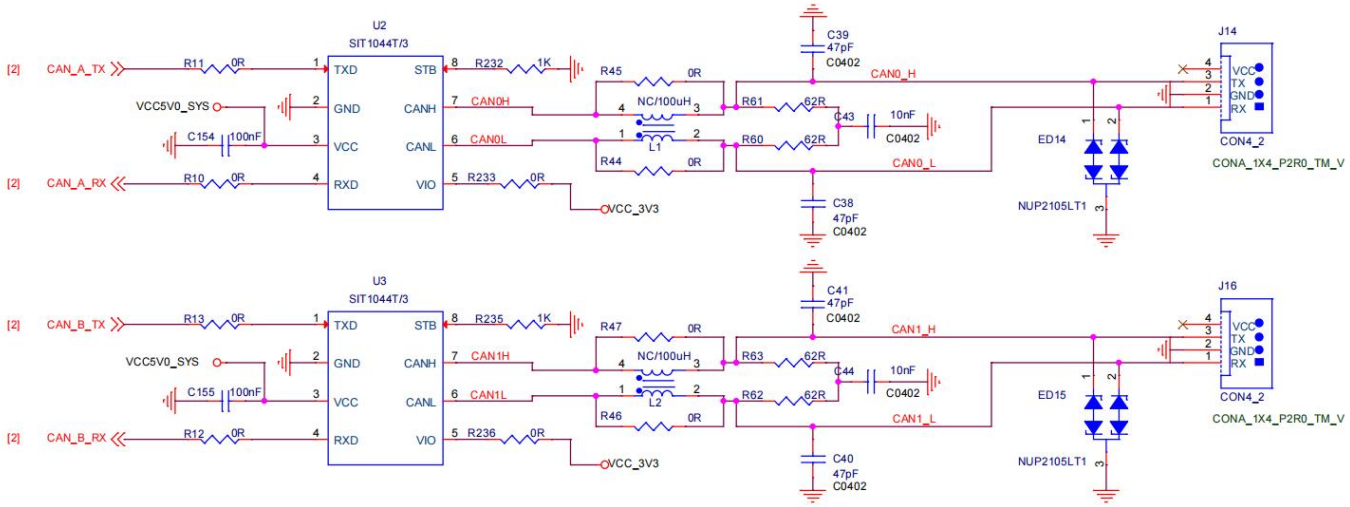
The development board is designed supporting 2 CAN channels, which is convenient for users to evaluate related functions.




CAN interface schematic

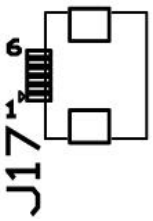
### 6.13.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J14 | 1 | CAN0_L | CAN0_L | |
| | 2 | Ground signal | GND | |
| | 3 | CAN0_H | CAN0_H | |
| | 4 | NC | NC | |
| J16 | 1 | CAN1_L | CAN1_L | |
| | 2 | Ground signal | GND | |
| | 3 | CAN1_H | CAN1_H | |
| | 4 | NC | NC | |



## 6.14 I2C Touch Panel Interface（J17）

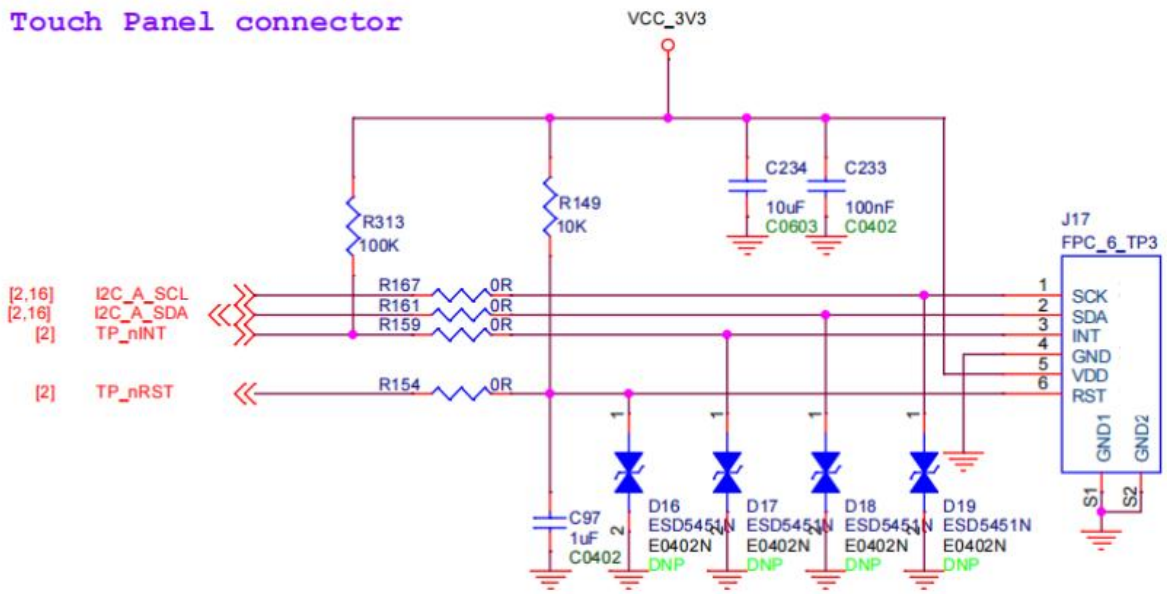
Designed all the way I2C capacitive touch screen interface, can be connected to capacitive touch screen, the development board system driver has been configured as a seven-inch capacitive touch screen




I2C Capacitive touch screen interface schematic

### 6.14.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J17 | 1 | I2C_A Clock | I2C_A_SCL | |
| | 2 | I2C_A Data | I2C_A_SDA | |
| | 3 | Touch screen Interrupt | TP_nINT | |
| | 4 | Ground signal | GND | |
| | 5 | 3.3V Power supply | VCC_3V3 | |
| | 6 | Touch screen reset | TP_nRST | |



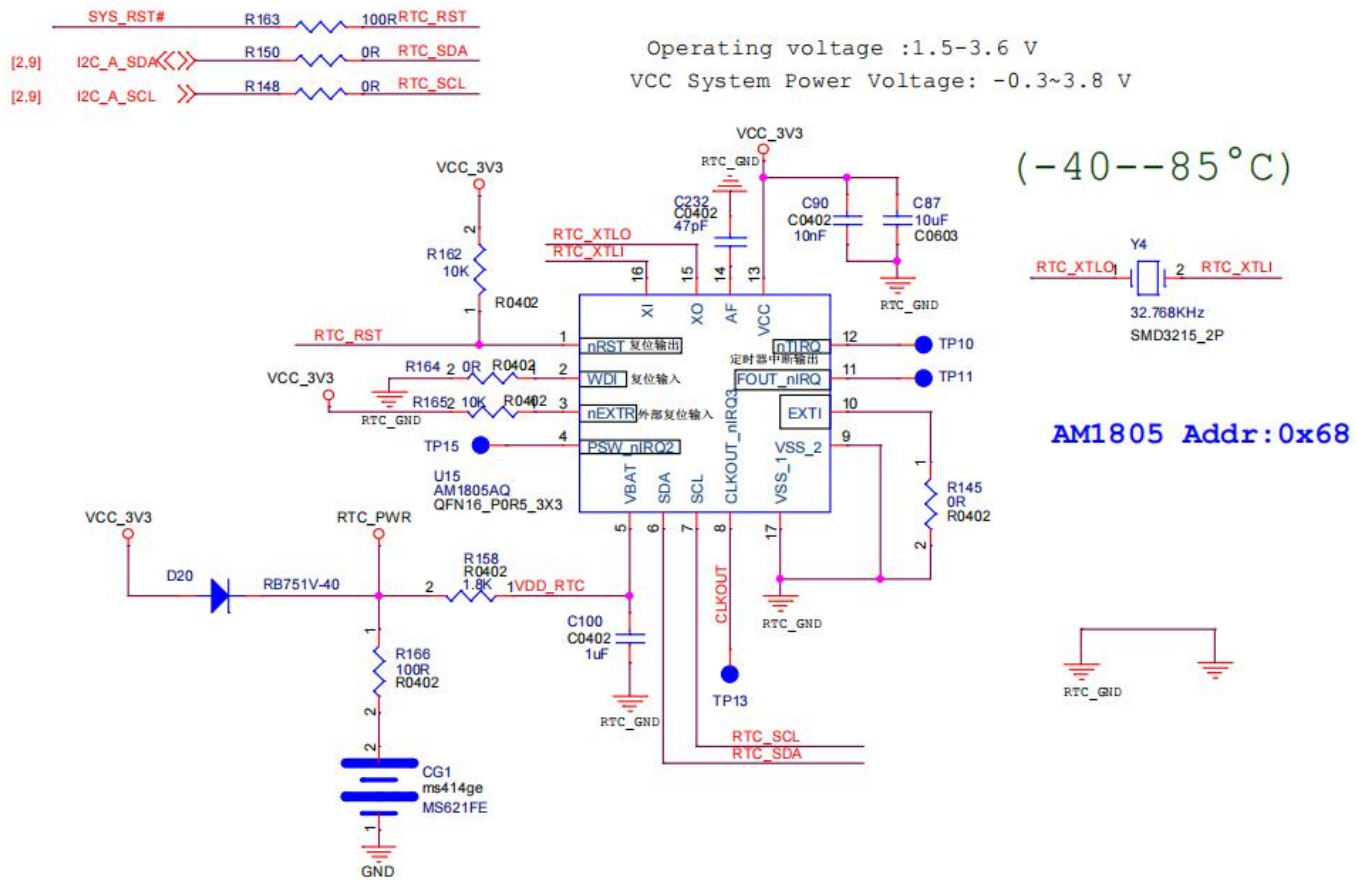
## 6.15 RTC Battery（CG1）

Design a rechargeable 3V RTC battery.


RTC 3V battery

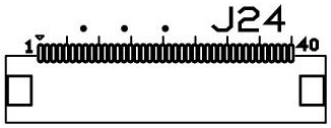
### 6.15.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| CG1 | 1 | Power ground | - | MS621FE |
| | 2 | RTC power supply 3V | - | |




## 6.16 DSI Interface（J24）

Designed a DSI interface, can be connected to the MIPI DSI interface model WD101HKM40AB-E6-05/HK101TLEDM-KM01 display, the maximum resolution of 1920 * 1080.

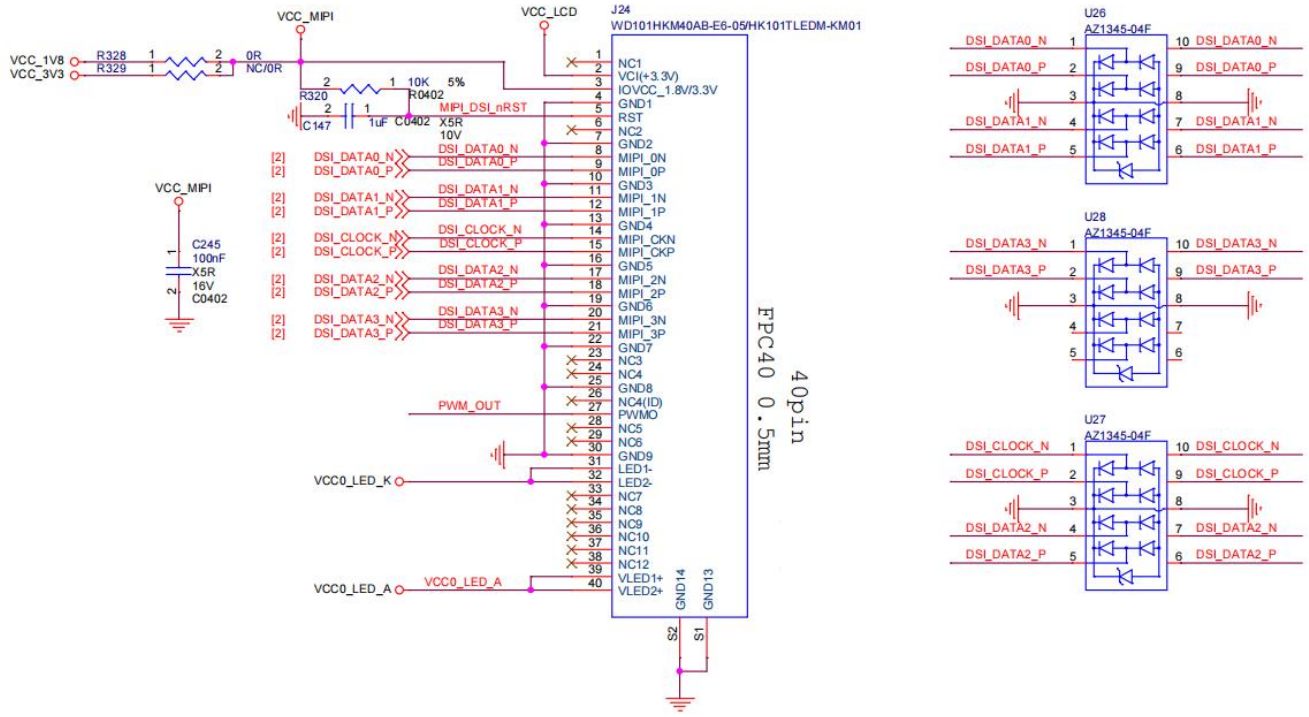


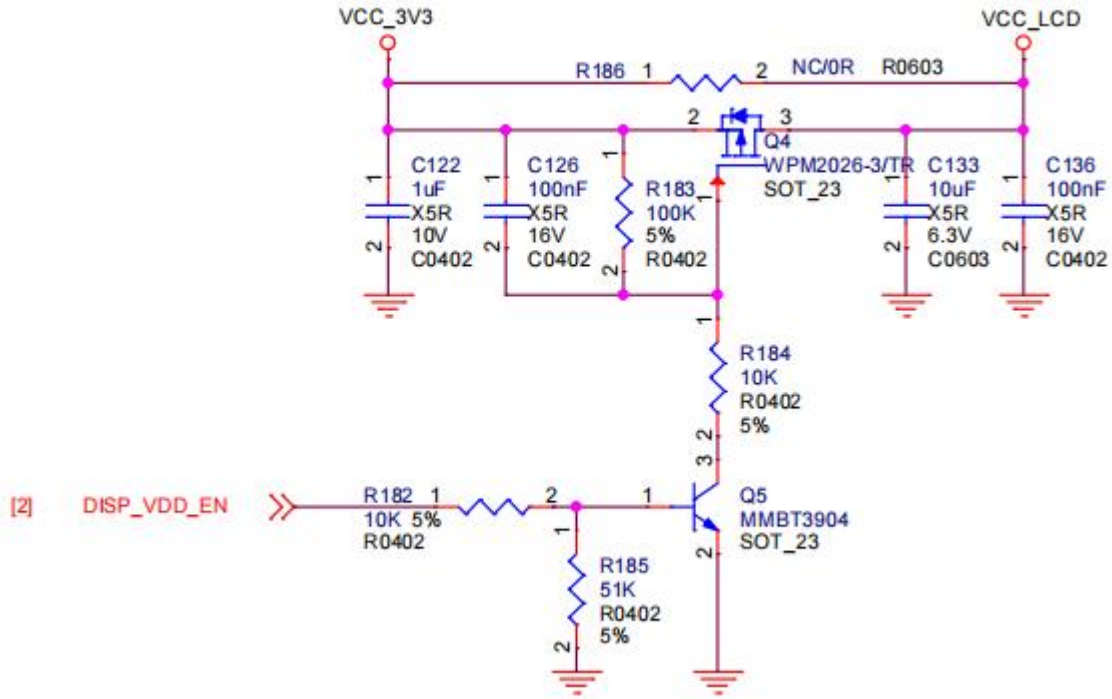

MIPI DSI display interface schematic

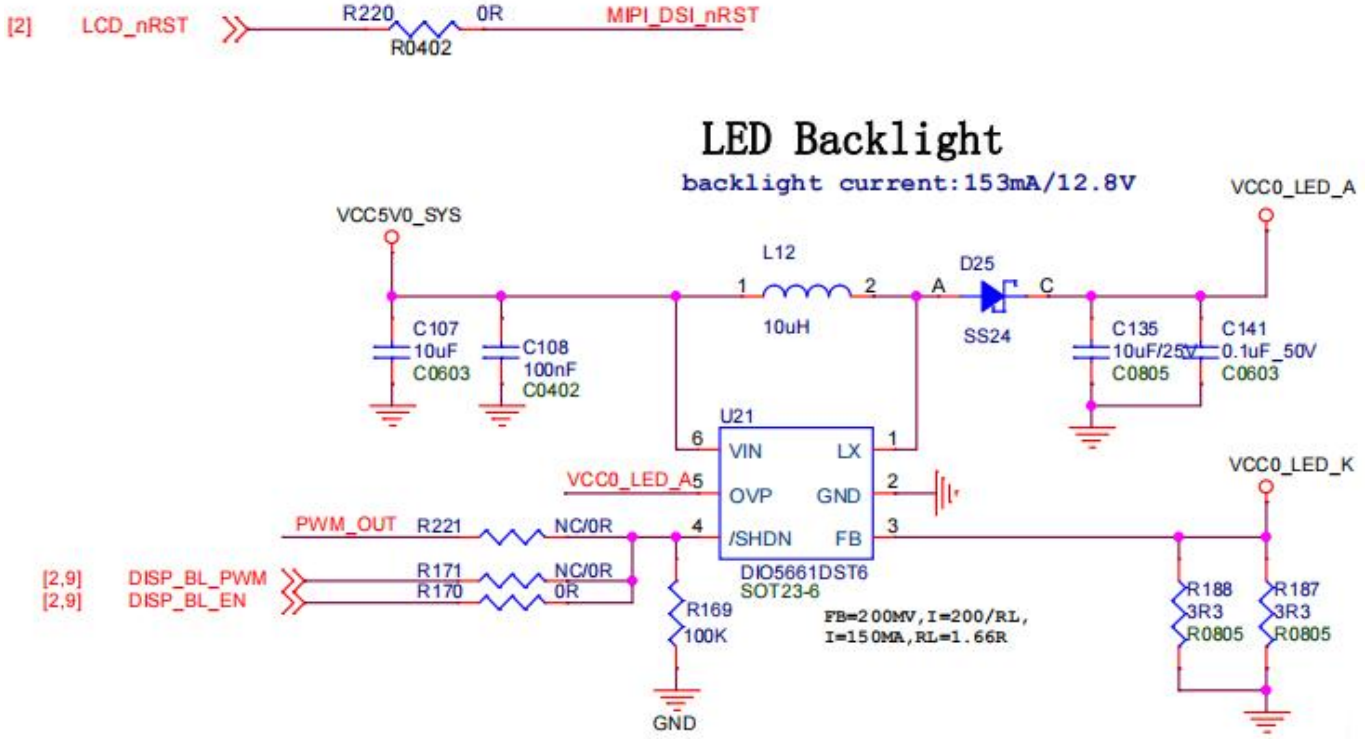
### 6.16.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J24 | 1 | NC | NC | |
| | 2 | Power supply 3.3V | VCC_LED | 3.3V |
| | 3 | Power supply 1.8V/3.3V | VCC_1V8/3V3 | 1.8V/3.3V |
| | 4 | Ground signal | GND | |
| | 5 | DSI reset signal | MIPI_DSI_nRST | |
| | 6 | NC | NC | |
| | 7 | Ground signal | GND | |
| | 8 | DSI interface data 0- | DSI_DATA0_N | |
| | 9 | DSI interface data 0+ | DSI_DATA0_P | |
| | 10 | Ground signal | GND | |
| | 11 | DSI interface data1- | DSI_DATA1_N | |
| | 12 | DSI interface data1+ | DSI_DATA1_P | |
| | 13 | Ground signal | GND | |
| | 14 | DSI interface clock- | DSI_CLOCK_N | |
| | 15 | DSI interface clock+ | DSI_CLOCK_P | |
| | 16 | Ground signal | GND | |
| | 17 | DSI interface data2- | DSI_DATA2_N | |
| | 18 | DSI interface data2+ | DSI_DATA2_P | |
| | 19 | Ground signal | GND | |
| | 20 | DSI interface data3- | DSI_DATA3_N | |
| | 21 | DSI interface data3+ | DSI_DATA3_P | |
| | 22 | Ground signal | GND | |
| | 23 | NC | NC | |
| | 24 | NC | NC | |
| | 25 | Ground signal | GND | |
| | 26 | NC | NC | |
| | 27 | | PWM_OUT | |
| | 28 | NC | NC | |
| | 29 | NC | NC | |
| | 30 | Ground signal | GND | |
| | 31 | LED backlight power supply- | VCC0_LED_K | |
| | 32 | LED backlight power supply- | VCC0_LED_K | |
| | 33 | NC | NC | |
| | 34 | NC | NC | |
| | 35 | NC | NC | |

| | | | | |
|---|---|---|---|---|
| | 36 | NC | NC | |
| | 37 | NC | NC | |
| | 38 | NC | NC | |
| | 39 | LED backlight power supply+ | VCC0_LED_A | |
| | 40 | LED backlight power supply+ | VCC0_LED_A | |

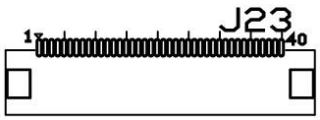





## 6.17 RGB LCD Interface（J23）

Provides a RGB LCD interface, can be connected to the RGB 24bit display, the maximum resolution of WVGA (1280 * 800)



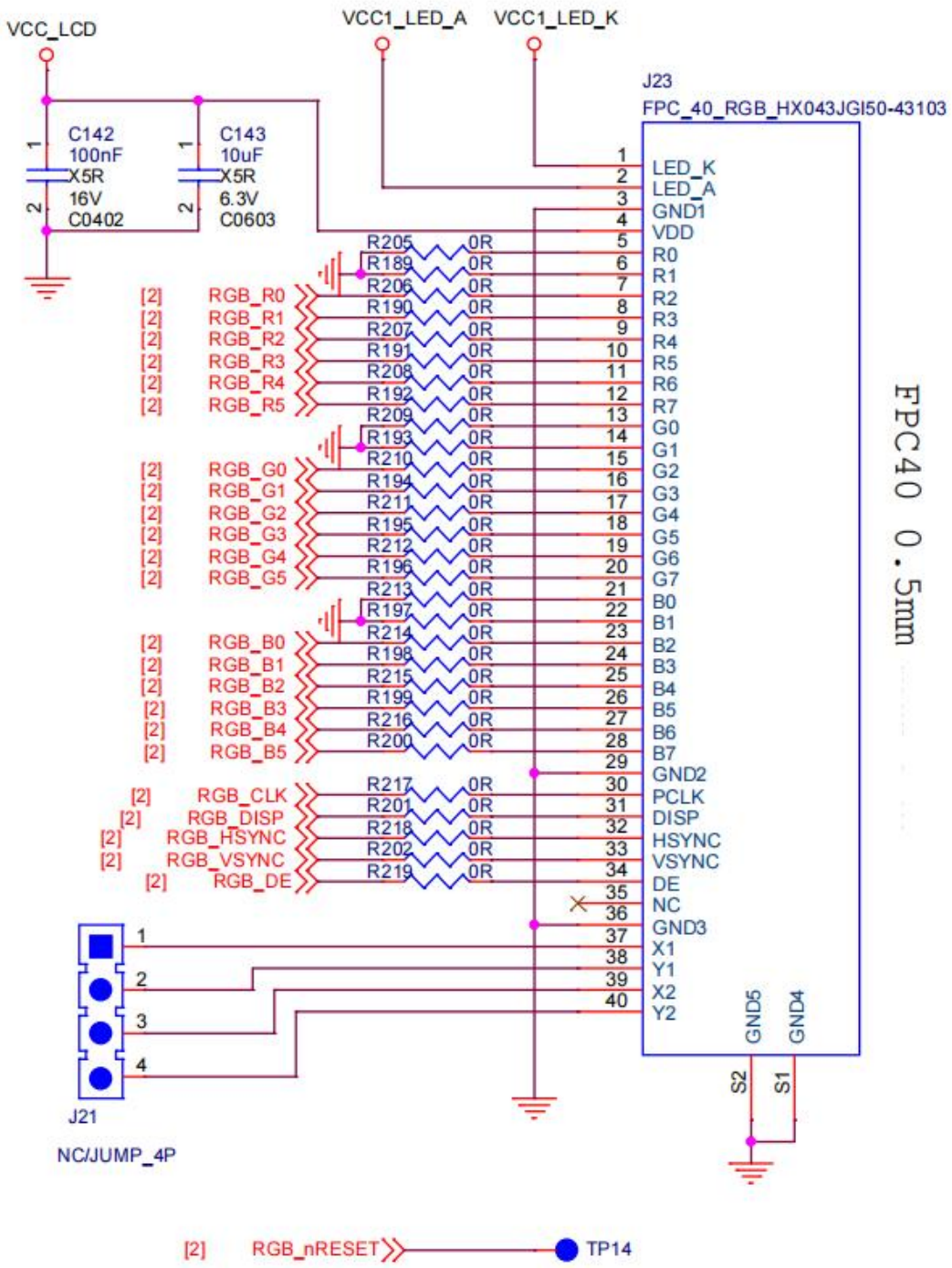

RGB LCD interface schematic

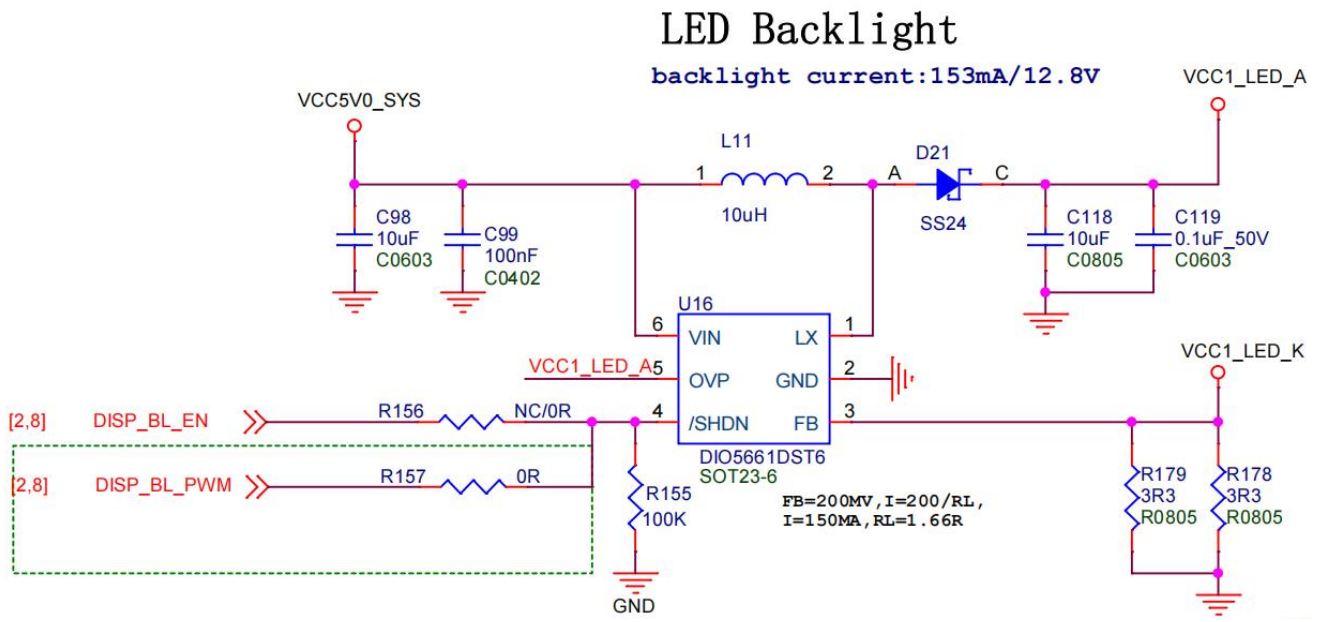
### 6.17.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J23 | 1 | Backlight LED Ground | VCC1_LED_K | 12.8V/153mA |
| | 2 | Backlight LED Power | VCC1_LED_A | |
| | 3 | Ground signal | GND | |
| | 4 | Power supply 3.3v | VCC_LCD | |
| | 5 | Ground signal | GND | |
| | 6 | GND signal | GND | |
| | 7 | Red data bus 0 | RGB_R0 | |
| | 8 | Red data bus 1 | RGB_R1 | |

| | | | | |
|---|---|---|---|---|
| | 9 | Red data bus 2 | RGB_R2 | |
| | 10 | Red data bus 3 | RGB_R3 | |
| | 11 | Red data bus 4 | RGB_R4 | |
| | 12 | Red data bus 5 | RGB_R5 | |
| | 13 | Ground signal | GND | |
| | 14 | Ground signal | GND | |
| | 15 | Green data bus 0 | RGB_G0 | |
| | 16 | Green data bus 1 | RGB_G1 | |
| | 17 | Green data bus 2 | RGB_G2 | |
| | 18 | Green data bus 3 | RGB_G3 | |
| | 19 | Green data bus 4 | RGB_G4 | |
| | 20 | Green data bus 5 | RGB_G5 | |
| | 21 | Ground signal | GND | |
| | 22 | Ground signal | GND | |
| | 23 | Blue data bus 0 | RGB_B0 | |
| | 24 | Blue data bus 1 | RGB_B1 | |
| | 25 | Blue data bus 2 | RGB_B2 | |
| | 26 | Blue data bus 3 | RGB_B3 | |
| | 27 | Blue data bus 4 | RGB_B4 | |
| | 28 | Blue data bus 5 | RGB_B5 | |
| | 29 | Ground signal | GND | |
| | 30 | Data clock signal | RGB_CLK | Fro controlling data transfer |
| | 31 | Standby mode select | RGB_DISP | |
| | 32 | Line SYNC signal | RGB_HSYNC | For controlling the horizontal synchronization of images |
| | 33 | Frame SYNC signal | RGB_VSYNC | For controlling the vertical synchronization of the image |
| | 34 | Data enable input | RGB_DE | |
| | 35 | NC | NC | |
| | 36 | Ground signal | GND | |

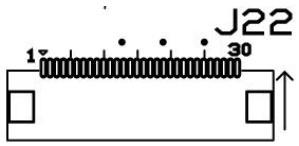
| | | | | |
|---|---|---|---|---|
| | 37 | NC | NC | |
| | 38 | NC | NC | |
| | 39 | NC | NC | |
| | 40 | NC | NC | |






## 6.18 CSI Camera Interface（J22）

Designed with a MIPI CSI camera interface, FPC interface for CSI_ZH13850-ZH-001 model cameras.

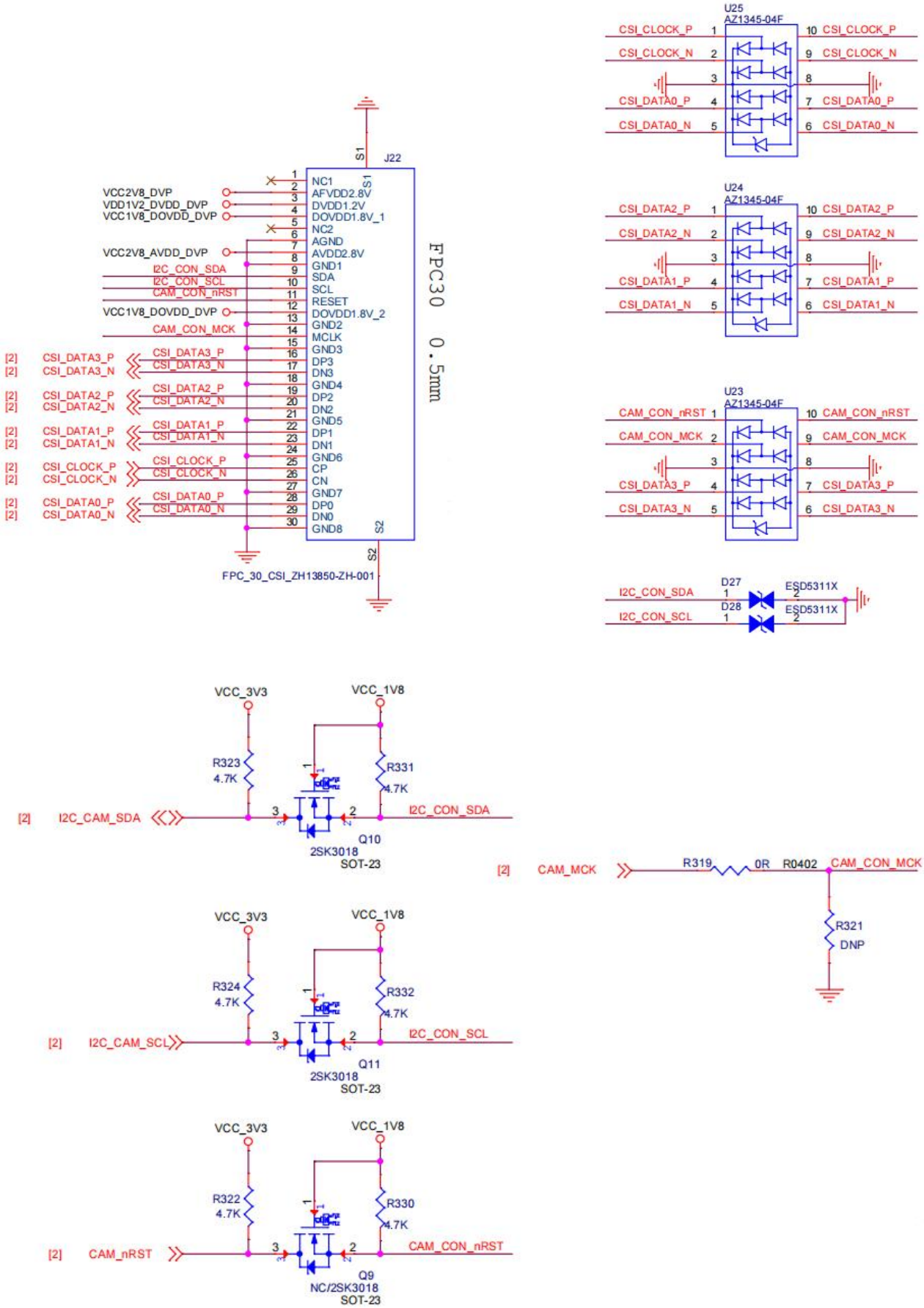


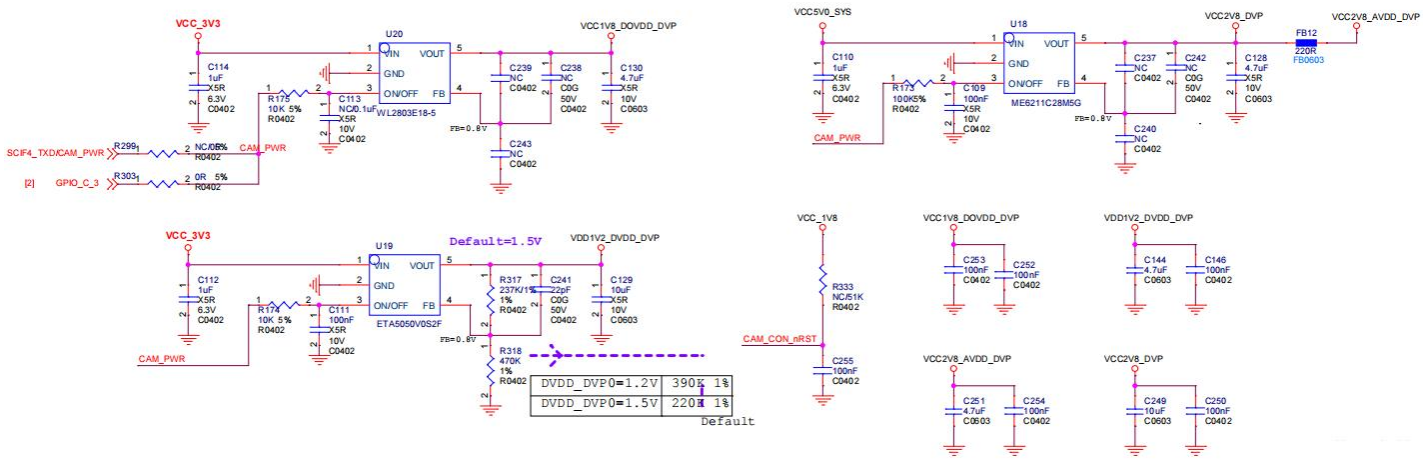

CSI Camera interface schematic

### 6.18.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J22 | 1 | NC | NC | |
| | 2 | Power supply 2.8V | VCC2V8_DVP | |
| | 3 | Power supply 1.2V | VDD1V2_DVDD_DVP | |
| | 4 | Power supply 1.8V | VCC1V8_DOVDD_DVP | |
| | 5 | NC | NC | |
| | 6 | Ground signal | GND | |
| | 7 | Power supply 2.8V | VCC2V8_AVDD_DVP | |
| | 8 | Ground signal | GND | |
| | 9 | I2C_CON data | I2C_CON_SDA | |

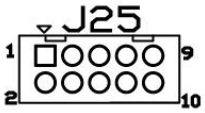
| | | | | |
|---|---|---|---|---|
| | 10 | I2C_CON clock | I2C_CON_SCL | |
| | 11 | Reset | CAM_CON_nRST | |
| | 12 | Power supply 1.8V | VCC1V8_DOVDD_DVP | |
| | 13 | Ground signal | GND | |
| | 14 | CSI master clock signal | CAM_CON_MCK | |
| | 15 | Ground signal | GND | |
| | 16 | CSI interface data 3+ | CSI_DATA3_P | |
| | 17 | CSI interface data 3- | CSI_DATA3_N | |
| | 18 | Ground signal | GND | |
| | 19 | CSI interface data 2+ | CSI_DATA2_P | |
| | 20 | CSI interface data 2 - | CSI_DATA2_N | |
| | 21 | Ground signal | GND | |
| | 22 | CSI interface data 1+ | CSI_DATA1_P | |
| | 23 | CSI interface data 1- | CSI_DATA1_N | |
| | 24 | Ground signal | GND | |
| | 25 | CSI interface clock+ | CSI_CLOCK_P | |
| | 26 | CSI interface clock- | CSI_CLOCK_N | |
| | 27 | Ground signal | GND | |
| | 28 | CSI interface data 0+ | CSI_DATA0_P | |
| | 29 | CSI interface data 0- | CSI_DATA0_N | |
| | 30 | Ground signal | GND | |


J22
FPC30 0.5mm
FPC_30_CSI_ZH13850-ZH-001
VCC2V8_DVP
VDD1V2_DVDD_DVP
VCC1V8_DOVDD_DVP
VCC2V8_AVDD_DVP
I2C_CON_SDA
I2C_CON_SCL
CAM_CON_nRST
VCC1V8_DOVDD_DVP
CAM_CON_MCK
CSI_DATA3_P
CSI_DATA3_N
CSI_DATA2_P
CSI_DATA2_N
CSI_DATA1_P
CSI_DATA1_N
CSI_CLOCK_P
CSI_CLOCK_N
CSI_DATA0_P
CSI_DATA0_N
U25
AZ1345-04F
U24
AZ1345-04F
U23
AZ1345-04F
D27
D28
ESD5311X
ESD5311X
VCC_3V3
VCC_1V8
R323
4.7K
R331
4.7K
I2C_CAM_SDA
I2C_CON_SDA
Q10
2SK3018
SOT-23
R324
4.7K
R332
4.7K
I2C_CAM_SCL
I2C_CON_SCL
Q11
2SK3018
SOT-23
R322
4.7K
R330
4.7K
CAM_nRST
CAM_CON_nRST
Q9
NC/2SK3018
SOT-23
CAM_MCK
R319
0R
R0402
CAM_CON_MCK
R321
DNP




## 6.19 System Extension Interface（J25）

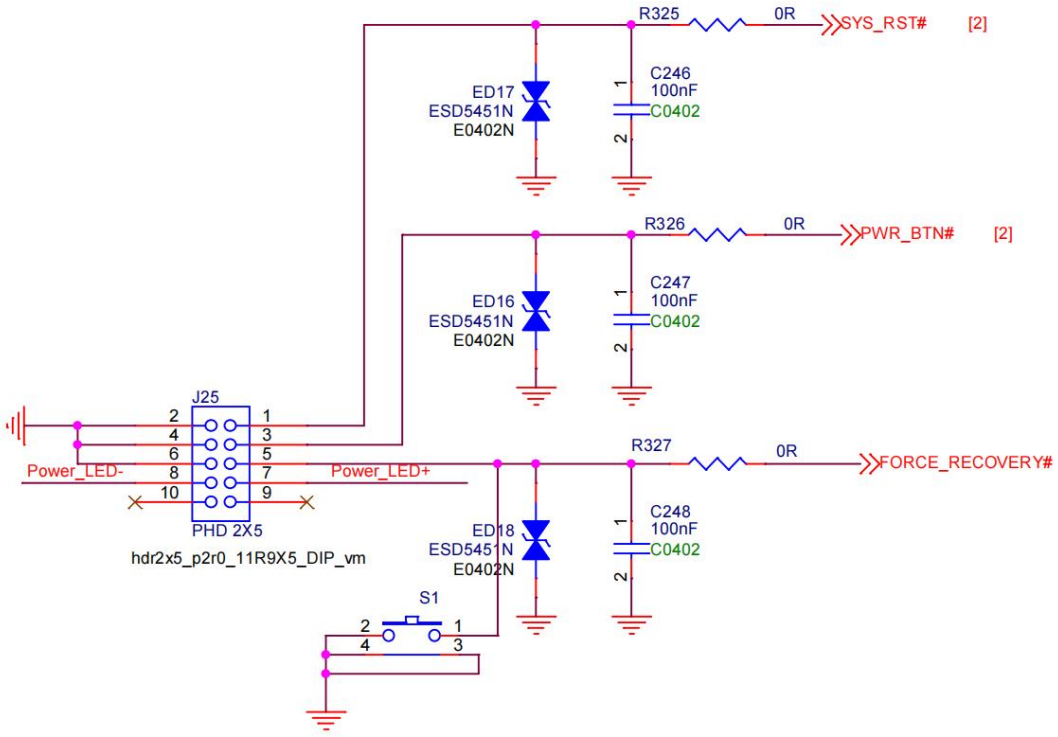
Designed a system expansion interface, can realize the connection of power indicator, power switch, reset button and other functions



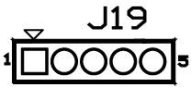

System extension interface schematic

### 6.19.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J25 | 1 | System reset | SYS_RST# | |
| | 2 | Ground signal | GND | |
| | 3 | Power switch | PWR_BTN# | |
| | 4 | Ground signal | GND | |
| | 5 | System Recovery | FORCE_RECOVERY# | |
| | 6 | Ground signal | GND | |
| | 7 | Power supply LED+ | Power_LED+ | |
| | 8 | Power supply LED+ | Power_LED- | |
| | 9 | NC | NC | |
| | 10 | NC | NC | |




## 6.20 PoE PD 12V Power Supply Output Interface(J19)

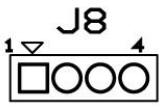



PoE PD 12V power supply output interface schematic

### 6.20.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J19 | 1 | Power Ground | GND | |
| | 2 | DC 12 + | VCC12_POE | |
| | 3 | NC | NC | |
| | 4 | DC12 + | VCC12_POE | |
| | 5 | Power Ground | GND | |

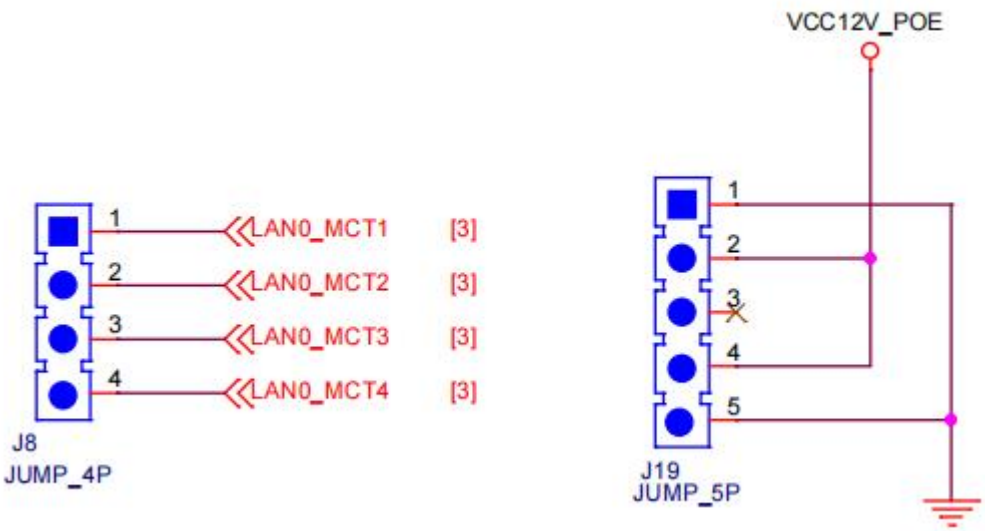
## 6.21 PoE PD Input Interface(J8)



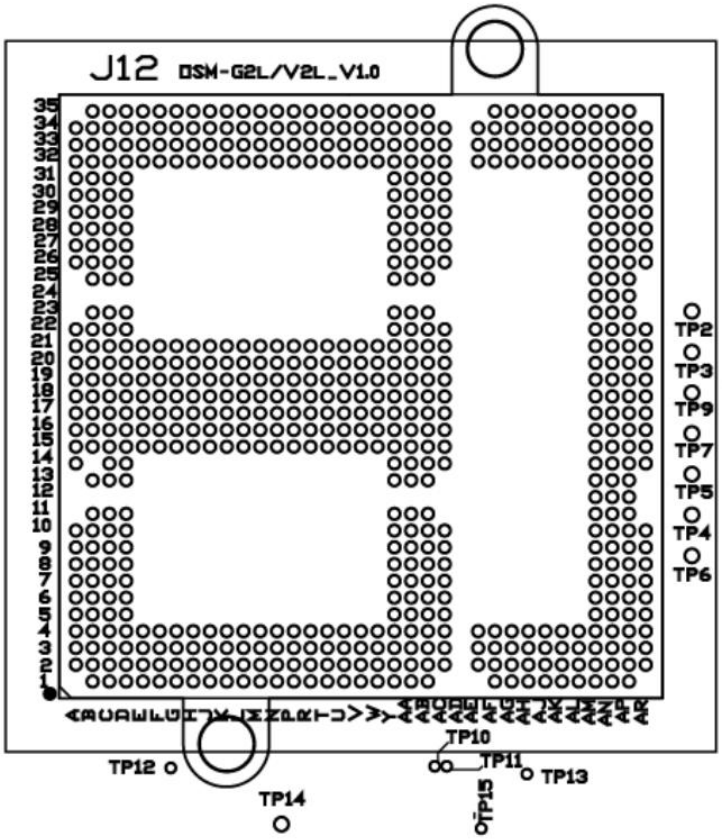

PoE PD Input interface schematic

### 6.21.1 Pin Definitions

| Label | Pin | Functional Description | Signal description | Remark |
|---|---|---|---|---|
| J8 | 1 | PoE Input 1 | LAN0_MCT1 | |
| | 2 | PoE Input 2 | LAN0_MCT2 | |
| | 3 | PoE Input 3 | LAN0_MCT3 | |
| | 4 | PoE Input 4 | LAN0_MCT4 | |



### 6.22 Core Board Module Interface（J12）




Core board module interface schematic

Refer to the OSM-G2L Core Board specification for pin definition.

## 7 Statements

This document provides information about the products of Shenzhen Geniatech Inc., Ltd, This document does not grant any license to any intellectual property rights, express or implied, or by estoppel or otherwise.

Shenzhen Geniatech Inc., Ltd assumes no liability other than that stated in the terms and conditions of sale of the products. And, the sale and/or use of the product without any express or implied warranty, including the product's fitness for a particular purpose, merchantability, or liability for infringement of any patent, copyright or other intellectual property rights, are not warranted.

Shenzhen Geniatech Inc.,Ltd products are not designed to be used for life-saving or life-supporting purposes, and Shenzhen Geniatech Inc., Ltd may make changes to product specifications and product descriptions at any time without notice.

Please contact the Shenzhen Geniatech Inc., Ltd sales office or distributor for the most up-to-date specifications before ordering products.

## More Help

Sales E-mail：sales@geniatech.com

Technical E-mail：support@geniatech.com

Technical Hotline：(+86)0755-8602-8588

Official Website：www.geniatech.com

Official Mall：https://shop.geniatech.com